An Online Evolvable Chebyshev Filter Based on Immune Genetic Algorithm

Wei Zhang, Yuanxiang Li and Nian Liu

***Abstract*—ANEHP-Alpha, a new analog evolvable hardware (EHW) platform based on AN231E04 field programmable analog array (FPAA) device is described and a fourth-order Chebyshev filter is evolved on it. AN231E04 is one of the latest models of the FPAA series based on switched capacitor technology from Anadigm Corporation. Reaping the benefit of its flexible dynamic reconfiguration ability and function-level design method, we can evolve more practical and larger-scale circuits. ANEHP-Alpha is a reliable intrinsic evolvable hardware platform with high performance. Immune genetic algorithm (IGA) is adopted to serve as the main evolutionary algorithm unit and a fast pre-evaluation and bad individual elimination method is employed, which highly increases the speed of evolution and ensures the devices against damage induced by illegal individuals. In the experiment, the evolved fourth-order Chebyshev filter acquires superior performance to that of classical ones, which shows the feasibility and efficiency of ANEHP-Alpha to design optimized practical analog systems.**

***Index Terms*—Chebyshev filter, EHW, FPAA, Immune genetic algorithm**

I. Introduction

The idea of self-recovering and self-reproduce machine was brought forward by John von Neumann in the mid twentieth century. But it was hard to be implemented due to the limitation of technical levels of that time. In 1992, Hugo de Garis put forward the concept of evolvable hardware (EHW) [1] which was the combination of evolutionary algorithm (EA) and reconfigurable circuit technology. A typical evolvable hardware system is composed of two main components: reconfigurable hardware and reconfiguration mechanism [2]. The reconfigurable hardware is the implementation and evaluation platform for EHW [3]. Reconfiguration mechanisms are usually certain branches of EA, such as Genetic Algorithm (GA) and Genetic Programming (GP).

Due to remarkable advances in recent CPUs and DSPs, applications with analog circuits are rapidly being replaced with digital computing. However, there are still many applications that require high-speed analog circuits. With challenging analog circuit design problems and fewer analog design engineers, there are economic reasons for automating the analog design process. The characteristics of analog circuits can vary widely due to environmental influences. In particular, component values (e.g. capacity and resistance) may vary by several tens of percent, due to changes in temperature. When an analog circuit is implemented as an integrated circuit, there are large variations in the values for components, caused by the manufacturing process or interference from other components. These variations impair the performance of the circuits, which can be especially serious when the specifications of the circuit require greater precision [4]. To solve these problems, analog EHW (especially the online mode) has become an important branch of evolvable hardware research and much valuable work has been done.

Analog EHW can be defined as hardware that is built on software-reconfigurable analogue circuits, and whose architecture can be reconfigured through genetic learning. Accordingly, the reconfigurable hardware technology is critical for it. The success of field programmable devices in the digital domain (FPGA and other "fine grain" programmable structures) has motivated some manufacturers to explore similar solutions to fast prototype in the Analog and mixed signal domains. Basically, the research in this area goes into two directions: One is the specialized analog integrated circuit with only limited programming capabilities. Leading manufacturer in this field is Lattice Semiconductors, makers of the inexpensive but relatively high-performance ispPAC family of programmable arrays, restricted mostly to continuous-time analog filters and lately also to mixed signal power supply controllers. The other one is the general purpose field programmable analog array (FPAA) [5] which can be regarded as the basic analog versions of FPGA. The dpAsp series of Anadigm Inc. ® is the most typical production of this type designed in switched-capacitor technology. In this research, we will use one of the latest productions of dpAsp series to fulfill our work.

In this paper, ANEHP-Alpha, a new analog intrinsic EHW platform based on AN231E04 FPAA device is described and a fourth-order Chebyshev filter is evolved on it. The paper is organized as follows. Section 2 introduces AN231E04, which is in the latest generation of the Anadigm dpAsp FPAA series. Section 3 describes the immune genetic algorithm (IGA) and the corresponding fitness function design. Section 4 introduces the whole system including the ANEHP-Alpha intrinsic EHW platform and the object circuit. Section 5 demonstrates the design of experiment and

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gives the results. Section 6 draws some conclusions.

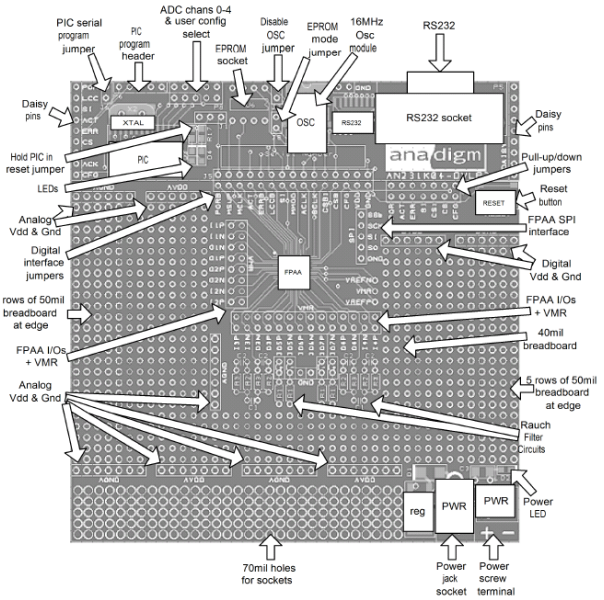

Fig.1 The layout of the AN231K04-DVLP3 development board.

II. Reconfigurable Analog Device AN231E04

According to the difference of implementation and evaluation strategy, EHW can be divided into three categories: extrinsic EHW (off-line evolution), intrinsic EHW (On-line evolution) and embedded EHW (On-Chip Evolution). Extrinsic EHW employs theorized model as the object circuit and software simulation as the method of evaluation [6]. It is a flexible method without considering the limitation of hardware type and exterior environments. But it consumes tremendous calculation and not suitable for evolution of analog circuits. On the contrary, intrinsic EHW is based on practical circuit implementation and hardware evaluation, which can be performed at high speed [7]. The process of intrinsic evolution is accomplished on the separated algorithm unit (usually a central computer) so that it can be easily controlled and cooperate with other related applications. Intrinsic EHW is a good choice for large-scale self-adaptive real time systems. The object circuit and algorithm of embedded EHW are implemented in the same chip so that it is fit for independent self-adaptive systems such as robots and embedded devices. In this work, the Chebyshev filter is evolved with the intrinsic method and its hardware implementation is based on a brand new reconfigurable analog device.

By the end of the last decade a new type of analog circuit, based on configurable blocks, was introduced to the market: the field programmable analog arrays. The FPAAs provide to the analog world the same advantages as their digital counterparts, the field programmable gate arrays, provide to digital circuits, such as reconfigurability and fast prototyping. This made it possible to implement intrinsic evolution for analog circuits, which had been regarded as one of the obstructions for EHW improvement. Among all kinds of FPAAs, the dpAsp series of Anadigm Inc. ® is the most typical production designed in switched-capacitor technology.

To develop intrinsic EHW in a dpAsp device, we employ the AN231K04-DVLP3 development board from Anadigm Inc. ® [8], which is the latest development kit production of this company. The layout of AN231K04 is shown in Fig.1. This board can be divided into three parts: 1) DpAsp chip, which is the most important component of the board, the analog circuit is configured by the program inside this chip and then the analog signal is processed here. 2) Digital interface, which is connected to PC through a RS232 CABLE. This interface is employed to download the configuration data to the chip and to control the course of signal processing. 3) Analog I/O interface. Analog signal is inputted and outputted through this interface.

The device on this development platform is an AN231E04, which is in the third generation of Anadigm FPAA series. It has a lot of advantages to its older counterparts. The most important one is the flexible dynamic reconfiguration ability. Old devices can be configured any number of times, but an intervening reset is required between each configuration load, so it is hard to develop any EHW application with these devices. AN231E04 is more flexible, allowing for 'on-the-fly' reconfiguration - that means we can reconfigure the device freely without reset. Furthermore, any configuration data can be downloaded in less than 15 ms and this high speed ensured the possibility to develop complex circuit.

The architecture of AN231E04 is shown in Fig.2. AN231E04 contains a 2x2 matrix of configurable analog blocks (CABs) which in turn can hold a number of predefined analogue functions provided as configurable analog modules (CAMs) with the Anadigm Designer 2 software installation. I/O capabilities are provided through two dedicated analogue Type1 I/O cells and two analog Type1A I/O cells as input or output. All this I/O cells can be programmed to satisfy the requirement of different I/O type. A Look up Table (LUT) is provided to build certain CAMs.

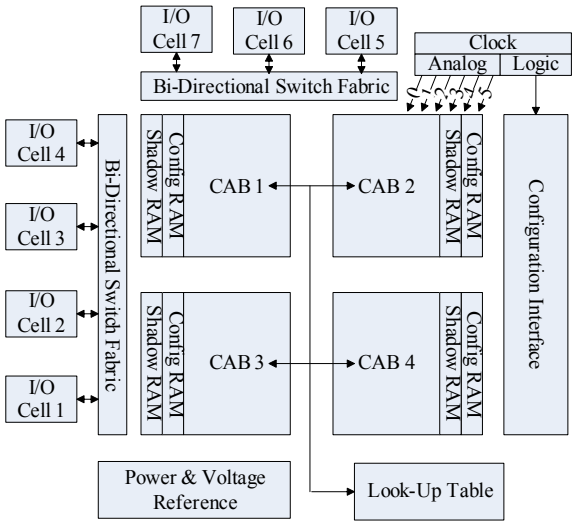

Fig.2 The architecture of AN231E04 dpAsp chip.

This device is based on switched capacitors technology. Switched capacitors circuits [9] are realized with the use of some basic building blocks, such as opAmps, capacitors, switches and non-overlapping clocks. The operation of these circuits is based on the principle of the resistor equivalence of

a switched capacitor [9]. This principle is illustrated in Fig.3, where φ_1 and φ_2 are the non-overlapping clocks. In Fig.3–(a), the average current is given by:

$$I_{avg} = C_1(V_1 - V_2)/T . \quad (1)$$

In (1), T is the clock period. This is equivalent to the resistor *Req*, shown in Fig.3–(b). With this technology, integrators, filters, and oscillators can be implemented.

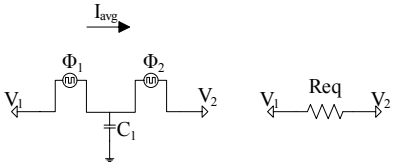

Fig.3 Switched capacitor/resistor equivalence principle.

III. Immune Genetic Algorithm

Genetic Algorithm is search algorithms based on the mechanics of natural selection and natural genetics [10], which are gradient-free, parallel and are well adapted to handling complex and irregular solution spaces. GA operates by generating an initial random population of individuals and progressing to subsequent generations by applying genetic operators and rewarding more suitable individuals with a higher chance of supplying genetic material. They have been applied by many to the problem of optimization and other related fields.

But the convergence of the simple genetic algorithm (SGA) was not fit for applying in the on-line (intrinsic) evolution. In this paper, immune genetic algorithm (IGA) [11] is employed to serve as the main evolutionary algorithm unit.

A. Immune system and immune response

The immune system (IS) is a complicated biological system made up by organ, cell and molecule. It can identify "self / not self" stimulus, and can eliminate foreign material.

A series of reject reaction to the antigen is known as immune response. Firstly, antigen presenting cell (APC) processes the foreign antigen material, then offer antigen out of it. Secondly lymphocyte identifies the antigen, and through a series of chemic response, immune response is produced.

When accepting the antigen to stimulate for the first time, the IS replies Primary Response. When the system receive that antigen stimulate for the second time, Secondary Response will occur.

More quick response and higher fitness are two main features to the Secondary Response compared with Primary response.

B. Immune genetic algorithm

If the algorithm itself is regarded as an immune system, practical problems are regarded as invading antigen, problem's solution is comprehended as antibody, and the process of finding the optimum solution can be comprehended as the process of adjusting the antibody, then we can find that there are the surprising similar between the seeking to practical problem optimum course and immune mechanism of the living beings.

C. The Operation Process of the IGA

1) Affinity

Affinity means the similar degree between the two different things. Functional analysis space vector concept is introduced to compute the fitness. So the antigen function can be defined as follow:

$$D(x_i, x_j) = 1/(\int |f(x_i) - f(x_j)|\, dt) \quad (2)$$

Where x_i and x_j are two solutions of the N-dimension solution space, and f (x_i) and f (x_j) are two vectors of *Y* space.

The more similar antigens are, the larger value of the function is. Then antigen and antibody affinity function can also be defined as:

$$D(x) = 1/(\int |f(X_i) - y|\, \mathrm{d}t) \quad (3)$$

Antigen *y* is the reference vector in the *Y* space. The more similar between antigen and antibody, the larger value of that function are.

2) Vaccine inoculation

Vaccine is summarized by priori knowledge. It can be likely to increase fitness of the antibody. We can gain some feasible solutions of the practical problems. Those solutions are called remedial vaccine. We inject them into the initial generation, which can greatly quicken convergence of the algorithm. But that can also probably induce the premature convergence. In order to overcome premature convergence, three steps were adopted. Firstly we enhance the probability of mutation, which can be likely to jump out of the trip. Secondly through adjusting the density of the antibody, the selection probability of lower fitness antibody also can be enhanced. At last, after generating new generation, some random antibodies will be injected into the new generation.

IV. The Intrinsic EHW Platform and Object Circuit

AN231E04 uses configurable analog modules (CAMs) rather than basic analog components such as resistors and transistors as its basic design element. This is an important advantage. Since anadigm's EDA tool Anadigm Designer 2 has offered a lot of various CAM models which are designed by highly experienced analog circuit engineers and tested strictly for hundreds of times, almost all predefined CAMs can offer perfect performance. Therefore, we can place more attention on evolving more practical and large-scale circuits by modifying the connection and sizing of CAMs. In this sense, AN231E04 is more appropriate than FPTA to develop EHW applications.

The work in this paper is a part of analog EHW platform section in No. 2007AA01Z290 Project of Chinese National High-Tech Research and Development Program (863 Program). As the experimental basis of this project,

ANEHP-Alpha, A high-speed intrinsic EHW platform for large-scale analog circuit based on AN231E04 has been defined. The whole platform is composed of mainly three parts: Computer, AN231K04-DVLP3 development board and external A/D circuit. In this work, a fourth-order Chebyshev filter will be evolved on ANEHP-Alpha.

A. Chebyshev Filter

The main object circuit to be evolved is a fourth-order Chebyshev filter. A typical one is shown in Fig.4. Here we can see that the fourth-order filter can be realized by stacking two sections of bi-quad filter vertically. The amount of bias current *I*, drawn from the supply voltage by the voltage reference and filter networks is usually unchanged. The only additional power is in **the** Q-controller gm_3, and gm_4.

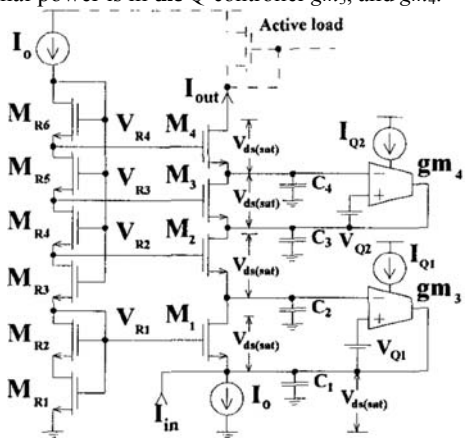

Fig.4 The schematic circuit diagram of typical fourth-order Chebyshev low-pass filter

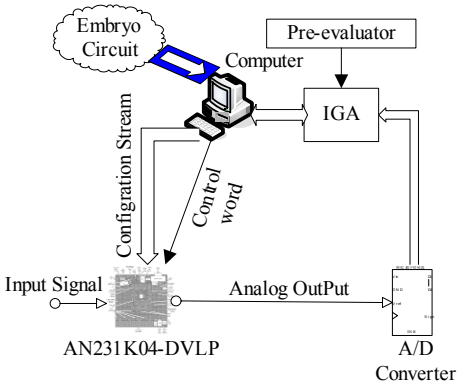

Fig.5 Intrinsic analog EHW platform ANEHP-Alpha

B. ANEHP-Alpha EHW platform

As the experimental basis of this project, ANEHP-Alpha is a high-speed intrinsic EHW platform for large-scale analog circuit based on AN231E04. The whole platform (Fig.5) is composed of three main parts and several assistant modules:

Computer. Computer is employed to generate the initial embryo circuit and fulfill the evolution algorithm. Anadigm Inc. has offered powerful EDA tool Anadigm Designer 2 for its dpAsps with the ability to create embryo circuit, simulate with embedded signal generator and create c++ code prototype for dynamic configuration.

AN231K04. AN231K04-DVLP3 development board can actually run each individual circuit during the course of evolution. But in practice, not all individuals are downloaded to development board out of consideration for evolution speed.

A/D Converter. The external A/D circuit transforms the analog output of AN231K04-DVLP3 development board into digital signal and feeds it back to the computer in order that the fitness of circuit individuals can be calculated. We employed AD673 8-Bit A/D converter produced by Analog Devices Inc. ® to fulfill this work.

IGA. The main evolutionary algorithm unit, where immune genetic algorithm is performed to search optimized circuit.

Pre-Evaluator. We employ some tricks of high speed pre-evaluate to find out the individuals which may present awful fitness or even injure the dpAsp chip. The program eliminates these individual from the download array and set their fitness to worst.

V. Design of Experiments and Results

A. Embryo Circuit

The intrinsically evolved Chebyshev filter is composed of three kinds of basic components: amplifiers, capacitors and programmable switch arrays. According to document [12], we designed its embryo circuit as Fig.6. As the initial state circuit, every three amplifiers and two capacitors compose a single evolvable module [12]. The parameters of this circuit are set to the basic safe value and will be decided by the binary configuration streams downloaded in the AN231E04 device during the course of evolution.

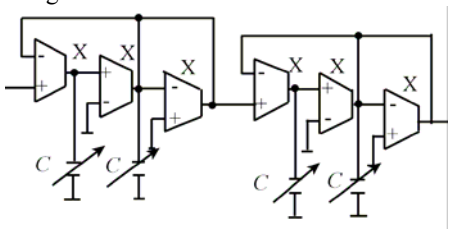

Fig.6 Embryo circuit of fourth-order Chebyshev filter

B. Fitness Evaluation

Fig.6 shows that the fourth-order Chebyshev filter is of a two-level structure and each level is a second-order low pass filters. If a fourth-order Chebyshev filter with 1000 Hz cut-off frequency and 0.5 dB ripple is to be designed, the parameters of the two levels should be set as following:

Level 1. Cut-off frequency: fc_1 = 1031.504 Hz; quality factor Q_1 = 2.939; damped coefficient $\zeta_1 = 1/2Q_1 = 0.170$.

Level 2. Cut-off frequency: fc_2 = 596.657 Hz; quality factor Q_2 = 0.706; damped coefficient $\zeta_2 = 1/2Q_2 = 0.708$.

Suppose that for the whole fourth-order filter, cut-off frequency is fc, gain is $K = 1$, and damped coefficient ζ, for each chromosome of the circuit, we can calculate its parameters: $fc_{1,}\zeta_{1,}fc_{2,}\zeta_2$ and then the fitness function (4) is employed as the evaluation criterion of individual circuits:

$$\Phi(fc_{1i}, fc_{2i}) = \sqrt{(fc_{1i}, fc_1)^2 + (fc_{2i}, fc_2)} \qquad (4)$$

C. Result

Fig.7 shows the amp-freq response. This figure indicates

that the evolved circuit has acquired satisfying performance. The parameters are adjusted with high precision, the response curves are very close to ideal values and almost all components including the amplifiers have actually participated in the evolution. The evolved circuit is compact with high value of theory and practice.

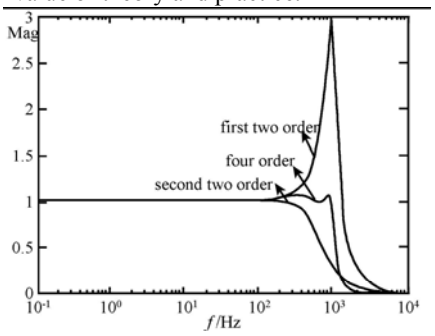

Fig.7 The amp-freq response of the evolved filter

Time performance is important for intrinsic EHW systems. Considering the requirements of practice, the criterion is set to converge within 3000 generation (about 14 minutes on ANEHP-Alpha). With the same initial state and different input signal, ten experiments are performed. As Table I shows, nine of ten have fulfilled this criterion and this result is acceptable for most online applications.

TABLE I. STATISTICS OF TIME CONVERGE AND RATIO OF ERROR

No.	Best Fitness	Convergence	Ratio of Error	Criterion Satisfied
01	2769.08	Y	0.0418%	Y
02	8015.34	Y	0.1207%	Y
03	4561.36	Y	0.0628%	Y
04	11857.09	Y	0.2183%	Y
05	5748.98	Y	0.0682%	Y
06	6847.78	Y	0.0749%	Y
07	21736.72	N	0.3935%	N
08	8935.21	Y	0.1305%	Y
09	3186.89	Y	0.0492%	Y
10	1895.89	Y	0.0294%	Y

VI. CONCLUSIONS

This paper demonstrates a fourth-order Chebyshev filter designed with immune genetic algorithm on intrinsic evolutionary hardware platform ANEHP-Alpha. This platform was constructed based on the AN231E04 dpAsp device, which is in the latest generation of the Anadigm dpAsp FPAA series. Reaping the benefit of AN231E04's flexible dynamic reconfiguration ability and function-level design method, we can evolve more practical and larger-scale circuits. IGA is employed as the main evolutionary method, which proved to be a good selection for intrinsic EHW systems. The evolved filter reveals superior performance to that of classical ones and the time performance is satisfying. The result of experiments shows that this system is adequate to the evolution of typical analog modules.

In future work, we will pay attention to the evolution of AN231E04's topology. We will try to find an appropriate encoding skill to realize combination code of connection and sizing. At the same time, we hope we can solve topology dynamic reconfiguration problem with Anadigm's help. We also plan to evolve more complex system such as multi-input controller and devices employed in extreme environments such as high or low temperature.

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