Low Power Full Adder Using 8T Structure

Amin Bazzazi, *Member, IAENG*, Alireza Mahini and Jelveh Jelini

***Abstract*— A low power and high performance 1-bit full adder cell is proposed. The 8T Full Adder technique has been used for the generation of XOR function. Twelve state-of-the-art 1-bit full adders and one proposed full adder are simulated with HSPICE using 0.18µm CMOS Technology at 1.8V supply voltage. By optimizing the transistor size in each stage the power and delay are minimized. The results of post-layout simulation compared to similar reported ones illustrate significant improvement. Simulation results show great improvement in terms of Power-Delay-Product (PDP). The power consumption of this adder is 200nw.**

***Index Terms*—Full Adder, Low Power, CMOS, Delay**

I. INTRODUCTION

INTEGER addition forms the basis of digital computer systems. Addition was found to be the most frequently encountered operation among a set of real time digital signal processing benchmarks in [1]. About 72% of the instructions of a prototype RISC machine, DLX resulted in addition/subtraction operations [2]. A study of the operations performed by an ARM processor's ALU revealed that additions constituted nearly 80% [3].

Historically, VLSI designers have used speed as the performance metric. High gains, in terms of performance and silicon area, have been made for Digital circuits. In general, small area and high performance are two conflicting constraints [4]. The power consumed for any given function in CMOS circuit must be reduced for either of the two different reasons: One of these reasons is to reduce heat dissipation in order to allow a large density of functions to be incorporated on an IC chip. Any amount of power dissipation is worthwhile as long as it doesn't degrade overall circuit performance. The other reason is to save energy in battery operated instruments same as electronic watches where average power is in microwatts

In CMOS circuits there are three types of power dissipation namely, the dynamic power dissipation, the short circuit power dissipation and the leakage power dissipation [5]. The average dynamic power dissipation of the CMOS logic gate, can be calculated from the energy required to charge down the total output load capacitance to ground level and charge up the output node to the V_{DD} driven by a periodic input voltage waveform with ideally zero rise and fall times. The total output of the dynamic power consumption is proportional to switching activity, capacitive loading and the square of the supply voltage [6].

The structure of the rest of this paper is organized as follows: Section II reviews twelve states of the full adder cells. In section III the Implementation of full adder with the 8T Technique is described. The simulation results are shown in section IV. Finally, section V contains the conclusion.

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II. REVIEW OF TWELVE STATE OF THE ART FULL ADDER CELLS

There are different types of CMOS full adder. This section reviewed the twelve state-of-the-art 1-bit full adders. This proposed cell is compared with them.

Twelve state of the art full adder cells are: 10T, 14T, CPL, TFA, TG CMOS, C^2MOS, Hybrid, Bridge, FA24T, N-Cell, DPL and Mod2f.

The first full adder structure in this section is 10T. It has only 10 transistors. The number of transistors is the advantage of this cell which leads to better performance and less silicon area. However poor driving capability and non full swing nodes are the serious problems of this full adder cell. The power consumption of this structure is 1.13µw.It is shown in fig. 1(a).

The 14T adder with 14 transistors consumes considerably less power in the order of microwatts and has higher speed. The 14T adder reduces threshold loss problem compared to the previous different types of transistor adders. In future, this kind of low power and high speed adder cell will be used in designing the digital FIR filter. The power consumption of this structure is 6.4µw. It is shown in fig. 1(b) [7].

The Complementary Pass-transistor Logic (CPL) full adder is shown in figure 1(c). This is contains the 18 transistors that based on NMOS pass-transistor network. This causes low input capacitance and high speed operation. Due to less output voltage swing that is the result of one Vt loss in the output, CPL consumes less power than standard static CMOS circuits. The power consumption of this structure is 2.5µw [7].

A Transmission Function Full Adder (TFA) based on the transmission function theory is shown in figure 1(d). It has 16 transistors. The power consumption of this structure is 12µw.

A Transmission- Gate Adder (TGA) is shown in figure 1(e). Transmission gate logic circuit is a special kind of pass-transistor logic circuit. It is built by connecting a

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PMOS transistor and an NMOS transistor in parallel, which are controlled by complementary control signals. Both the PMOS and NMOS transistors will provide the path to the input logic "1" or "0", respectively when they are turned on simultaneously. Thus, there is no voltage drop problem whether the "1" or "0" is passed through it. It contains the 20 transistors [8].

The Complementary CMOS full adder (C^2MOS) is shown in fig. 1(f) .The advantage of complementary CMOS style is its robustness against voltage scaling and transistor sizing which are essential to provide reliable operation at low voltage and arbitrary transistor. It contains the 28 transistors [8].

Hybrid Full Adder cell, which contains the 26 transistors, utilizes a modified low-power XOR/XNOR circuit. In this circuit worst case delay problems of transitions from 01 to 00 and from 10 to 11 are solved by adding two series PMOS and two series NMOS transistors respectively. The power consumption of this structure is 2.22µw. it is shown in fig. 1(g) [7].

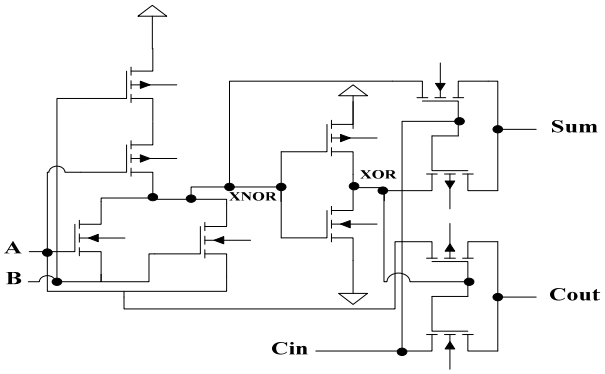
The Bridge circuit has 26 transistors which are shown in fig. 1(h). This design creates a conditional conjunction between two circuit nodes. Since one of the important parameters in circuit design is the chip area, the proposed style might reduce the area or increase density of transistors in this unit of area. The power consumption of this structure is 1.66µw [9].

The FA24T structure is shown in fig. 1(i). This full Adder is based on Bridge style. FA24T has 24 transistors. The body of FA24T has two transistors less than Bridge and has better power consumption. However, in FA24T the Sum generator should wait to receive the Cout signal from the Cout generator; therefore, the delay of FA24T is more than Bridge. The power consumption of this structure is 1.66µw [7].

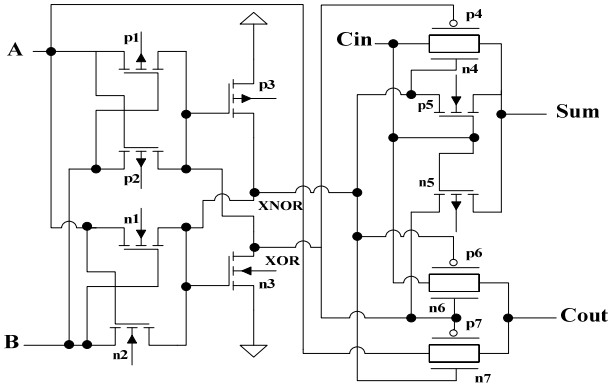
N-CELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit. There is a pass transistors network to produce a non full swing Sum signal and uses four transistors to generate a full swing Cout signal. However, NCELL Full Adder cell has 12 transistors less and better performance in comparison with Hybrid Full Adder cell. The power consumption of this structure is 1.62µw. It is shown in fig. 1(j) [10].

The Double Pass-transistor Logic (DPL) Full Adder of the fig. 1(k) is a modified version of CPL and contains the 24 transistors. Full swing operation is obtained by simply adding PMOS transistors in parallel with the NMOS transistors in DPL circuits. Therefore, the problems of little noise margin and performance degradation at low supply voltages, which occur in CPL circuits because of the output voltage drop, are avoided. However, the addition of PMOS transistors bring about increased input capacitances. The power consumption of this structure is 2.35µw [7].

Mod2f Full Adder cell of Fig. 1(l), which contains the 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. As mentioned in, this leads to higher speed and better performance in comparison with the circuit proposed. The power consumption of this structure is 2.23µw [7].



(1-a)



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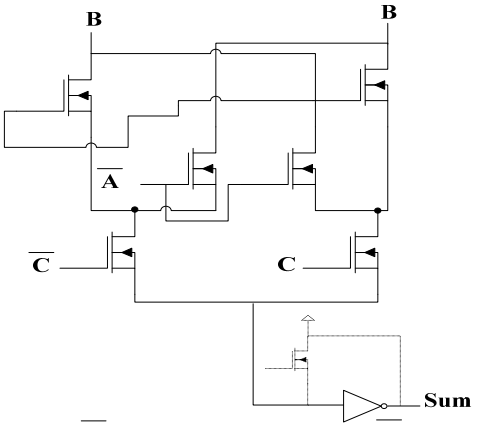

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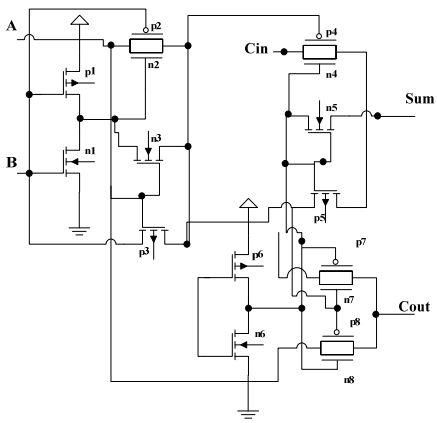

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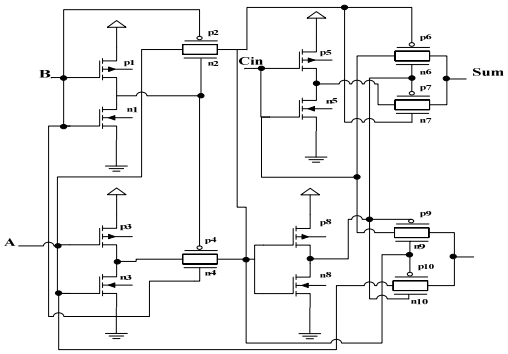

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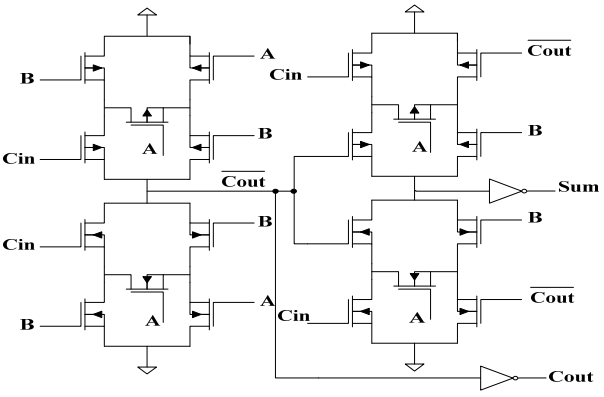

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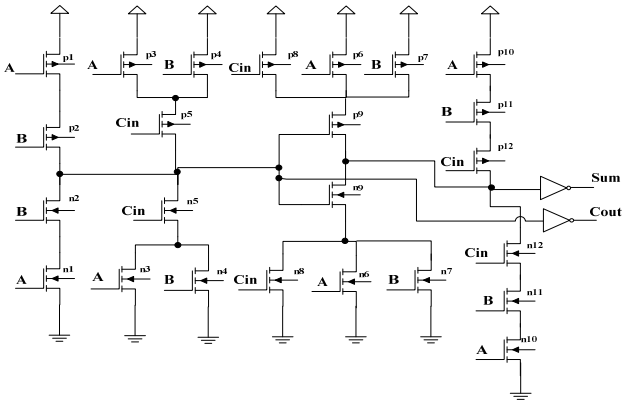

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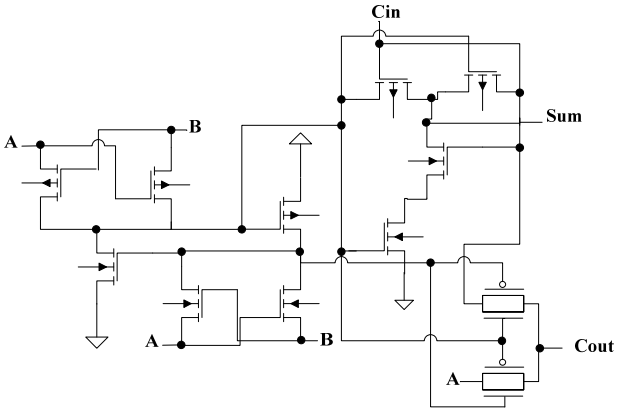

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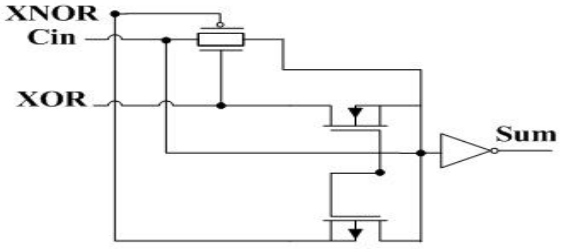
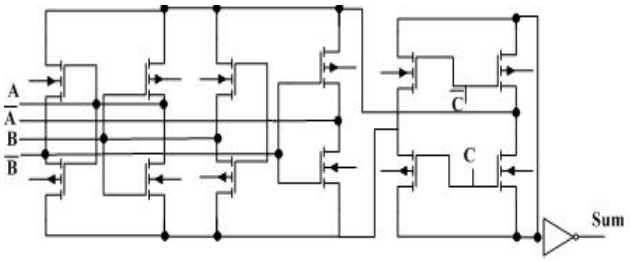


(1-g)



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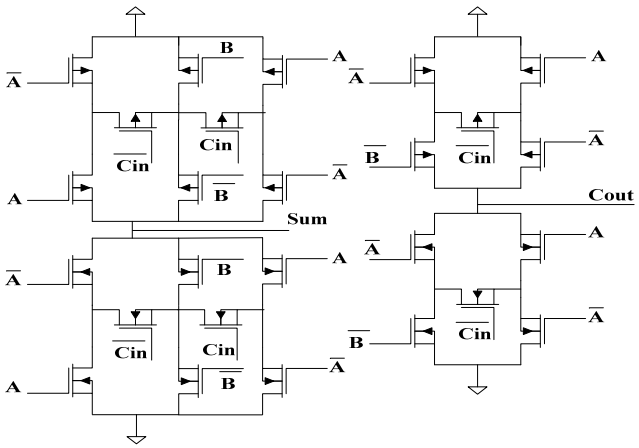
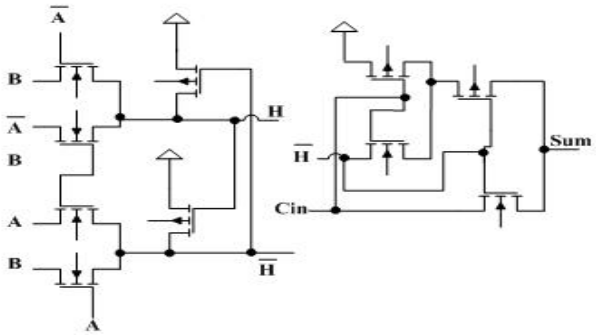


(1-h)



(1-l)

Fig.1- Twelve state of the art full adder cells .(a)10T, (b)14T, (c)CPL, (d)TFA, (e)TG-Cmos, (f)C^{2}mos, (g)Hybrid, (h)Bridge, (i)FA24T, (j)N-Cell, (k)DPL, (l)Mod2f.

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III. IMPLEMENTATION OF FULL ADDER CELLS

8T Full Adder method is based on the use of a simple cell as shown in fig. 2. XOR and XNOR functions are the key variables in adder equations. If the generation of them is optimized, this could greatly enhance the performance of the full adder cell. In this new cell has used 3 transistors for generating of XOR functions.

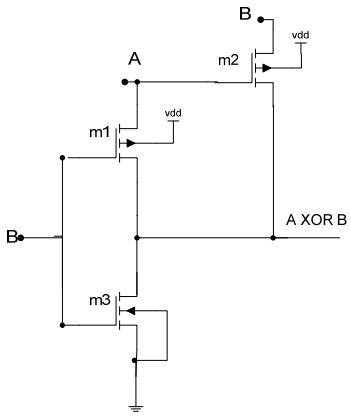

Fig. 2- 3T XOR basic cell

A one-bit binary full adder takes three one-bit inputs: A, B and Cin and generate sum and carry.

Sum= (A ⊕ B) ⊕ Cin)
Carry= A. B + Cin (A ⊕ B)

The goal of this paper is to design a high performance and low power full adder cell with the 8T method. The full adder cell is shown in Fig.3. Compared to the various structures, a typical Full Adder in 8T logic embodies only 8 transistors and the number of interconnections between them is highly reduced. Having each transistor a lower interconnection capacitance, the W/L can be close to the minimum value and the power consumption is decreased. The total input capacitance consists of the input node (in) and interconnection capacitance obtained by post-layout parasitic extraction, is 2 fF.

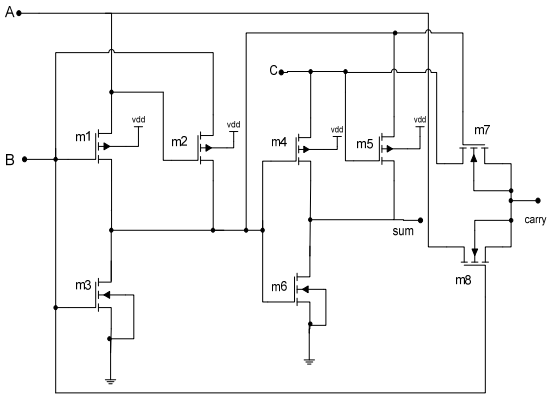

Fig. 3- The proposed full adder cell with 8T Structure

IV. SIMULATION RESULTS

The Full Adder operates in 100MHz range. Infact, in addition to normal transistors, circuits are tested in corner cases with fast and slow transistors and their combination, too. In each stage one of the components FF, SS, FS, SF are replaced instead of normal transistors in circuit and are perused circuit functions. The difference in this stage is in consumption power and falling and rising times so this subject looks simple due to the difference in nMOS and pMOS transistors speed. The layout of circuit is drawn and by the post simulation result a few correction, have achieved in sizes that the circuit has an accurate operation. The 5% variation of power supply and also several temperatures are measured. The supply have varied between 1.6 to 2 volt range and the temperature have varied in the -25, 25, 125 degree centigrade are tested. This design is also compatible with transistor size 10% variation. Output waveform is shown in figure 4. In the table I, comparison of similar works and their results has been there.

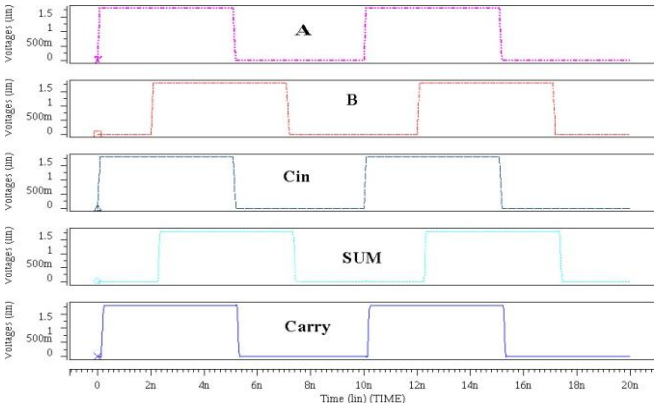

Fig.4- Snapshots of waveforms at 1.8V and 100MHZ.

Table I. Comparison of similar works (Power, Delay and Power-Delay-Product)

Structure	No. Transistors	Power (μw)	Delay (ns)	PDP (aj)
10T	10	1.13	73.5	83.05
14T	14	6.4	-	-
CPL	18	2.5	141.1	352.7
TFA	16	12	-	-
TGA	20	-	342	-
C^2MOS	28	-	364	-
HYBRID	26	2.22	80.6	178.9
FA24T	24	1.66	137.9	228.91
BRIDGE	26	1.66	104.2	172.97
N-CELL	14	1.62	63.2	102.3
DPL	24	2.35	75.3	176.95
MOD2F	26	2.23	87.7	195.57
This Work	8	0.02	200	40

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V. CONCLUSION

The aim of this work had been power reduction in the Full adder circuit. In this operation the 8T Adder is introduced. By using techniques such as size optimizing and using the buffer between the stages can reduce the power consumption. As a result the 8T adder works at the 100 MHz speed with 200nw power consumption. These results were obtained with spice simulation from the extracted net list of the layouts for normal parameters, room temperature and power supply at 1.8V.

The power was improved by 40% comparing to the 10T, by 70% to the Hybrid, by 58% to the Bridge, by 56% to the N-Cell and by 70% to the Mod2f.

The power delay product was improved by 25% comparing to the 10T, by 65% to the Hybrid, by 64% to the Bridge, by 37% to the N-Cell and by 68% to the Mod2f.

The power, delay and power product delay were improved. The result of this work and others are shown in Table I.

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