A High-Gain Serial-Parallel-Switched-Capacitor Coupled-Inductor Boost DC-AC Inverter

Yuen-Haw Chang and Zheng-Bin Li

***Abstract*—A closed-loop scheme of a high-gain serial-parallel-switched-capacitor coupled-inductor (SPSCCI) boost DC-AC inverter is proposed by combining a two-phase generator and sinusoidal pulse-width-modulation (SPWM) controller for low-power step-up DC-AC conversion and regulation. In this inverter, the power part is composed of SPSCCI booster and half-bridge DC-link. This booster is a 4-stage SC circuit plus combining a coupled-inductor, and it raises the voltage gain up to $[4(n+1)+(1+nD)/(1-D)]$ at most via two-phase operation, where D is the duty cycle and n is the turn ratio of coupled-inductor. The DC-link is a half-bridge circuit in order to convert the DC voltage into AC via SPWM control for realizing the range of sinusoidal output: $+0.5[4(n+1)+(1+nD)/(1-D)]V_S \sim -0.5[4(n+1)+(1+nD)/(1-D)]V_S$. Practically, the maximum output voltage can reach 26.0 times voltage of source V_S while D=0.5, n=4. Here, the SPWM is employed to enhance regulation capability for the different output amplitude and frequency, as well as robustness to source/loading variation. Finally, the closed-loop SPSCCI inverter is designed and simulated by SPICE for some cases: steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*—serial-parallel-switched-capacitor, coupled-inductor, high-gain boost, DC-AC inverter, sinusoidal pulse-width-modulation.**

I. Introduction

Recently, high-gain step-up power converters are widely used as power modules between the available low-voltage sources and the output loads, such as lighting device, smart phone, and medical equipment ...etc. These modules are always asked for some good characteristics: small volume, light weight, higher efficiency, and better regulation capability. Generally, the traditional converters have a large volume and a heavy weight due to magnetic elements. Therefore, more manufactures and researchers pay much attention to this topic, and ultimately, requiring DC-DC/DC-AC step-up converters realized on a compact chip by mixed-mode VLSI technology.

This kind of switched-capacitor (SC) power converters, containing only capacitors and MOSFET switches, is one of the good solutions to provide the higher voltage gain for realizing the boost DC-DC/DC-AC conversion in the non-magnetic circuit. Up to now, the various SC types have been suggested. In 1976, Dickson charge pumping was proposed based on a diode-chain structure via pumping capacitors [1]. In 1990s, Ioinovici proposed a SC with two capacitor cells working complementarily, as well as current-mode SC [2-3]. In 2007, Chang proposed a CPLD-based implementation of SC step-down DC-DC converter for multiple output choices [4]. In 2011-2013, Chang *et al*. proposed a series of multistage/multiphase SC step-up/down DC-DC/DC-AC converter/inverter [5-8]. In 2014, Chang *et al*. proposed a 2-stage 4-phase SC-based boost DC-AC inverter with sinusoidal PFM control [9]. In 2015, Chang *et al*. proposed a closed-loop high-gain switched-capacitor-inductor-based boost DC-AC inverter [10].

To obtain a higher voltage gain, it is one of the good ways by using the turn ratio and/or extra winding stage of the coupled-inductor. Nevertheless, the stress on transistors and the volume of magnetic device must be considered. In 2015, Chen *et al*. proposed a coupled-inductor boost integrated flyback converter including high-voltage gain and ripple-free input current [11]. Bahrami *et al*. suggested a modified step-up boost converter with coupled-inductor and super-lift techniques [12]. Chen *et al*. proposed a novel switched-coupled-inductor DC-DC step-up converter and its derivatives [13]. Wu *et al*. proposed a nonisolated high step-up DC-DC converter adopting switched-capacitor cell [14]. Nouri *et al*. proposed an interleaved high-gain step-up DC-DC converter based on three-winding high-frequency coupled-inductor and voltage-multiplier cell [15]. In 2016, Chang *et al*. proposed a novel coupled-inductor switched-capacitor inverter for high-gain boost DC-AC conversion [16]. Here, the authors make an attempt on combining 4-stage SC circuit with one coupled-inductor to propose a closed-loop SPSCCI inverter for the high-gain DC-AC conversion and regulation.

II. Configuration of SPSCCI Inverter

Fig. 1 shows the high-gain serial-parallel-switched-capacitor coupled-inductor (SPSCCI) inverter proposed, and it contains two major parts: power and control part achieving the boost DC-AC conversion and closed-loop regulation. These two parts are discussed as follows.

A. Power Part

The power part of this inverter as in the upper half of Fig. 1 contains a SPSCCI booster and a half-bridge DC-link in cascaded connection between supply V_S and output V_{OUT}.

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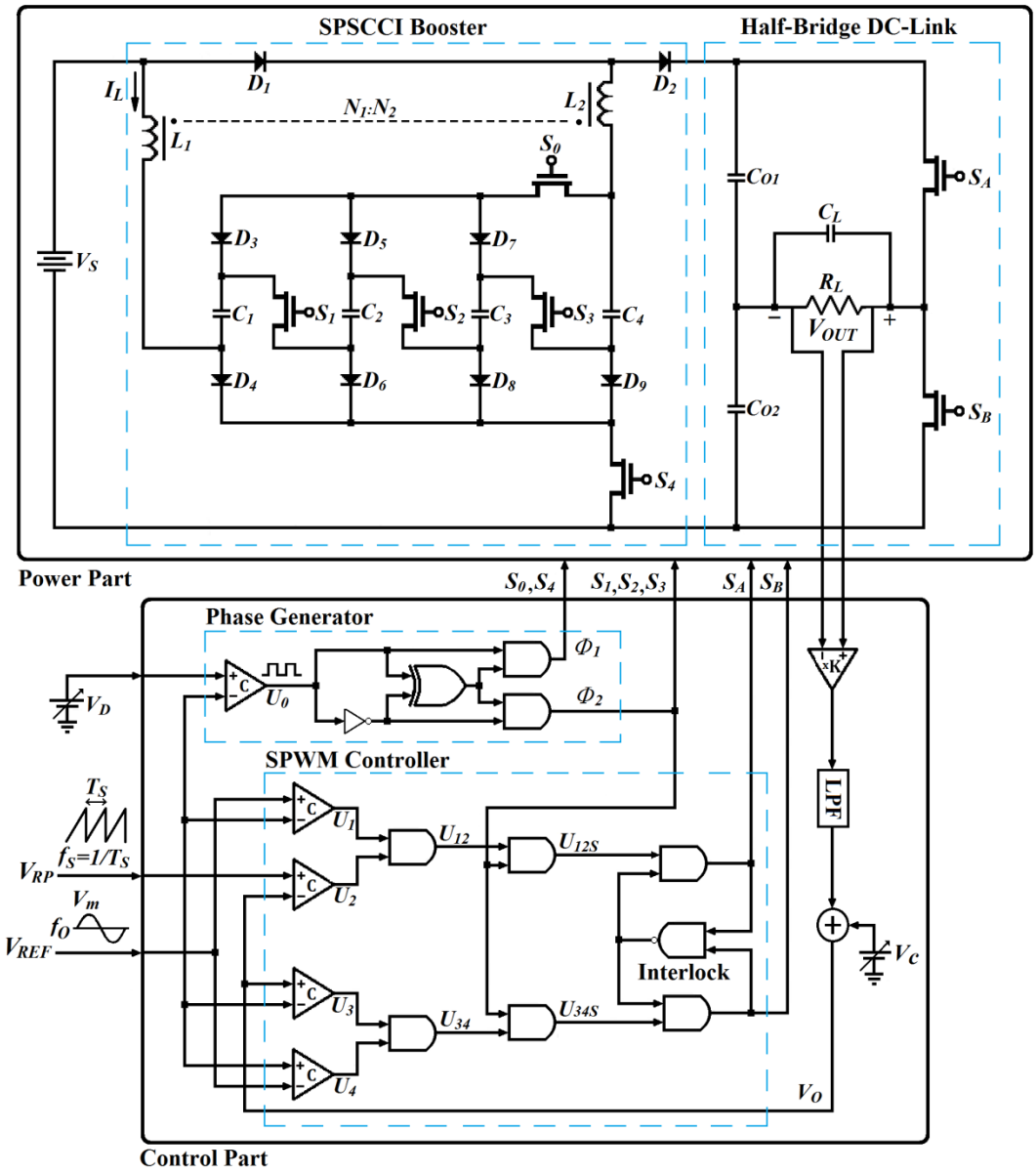

Fig. 1. Configuration of SPSCCI inverter.

Firstly, the SPSCCI booster is a 4-stage SC circuit plus combining a coupled-inductor. It includes switches S_0, S_1, S_2, S_3, and S_4, diodes D_1-D_9, coupled-inductors L_1, L_2, pumping capacitors C_1, C_2, C_3, and C_4, where it is assumed that same capacitance C (C_1=C_2=C_3=C_4=C). The coupled-inductor L_1 and L_2 is modeled as an ideal transformer with a turn ratio of n (n=N_2/N_1). The main function of this booster is to raise the voltage gain up to [4(n+1)+(1+nD)/(1-D)] at most from supply V_S to half-bridge total capacitor voltage (V_{CO1}+V_{CO2}), where D (0<D<1) is the duty cycle and DT_S is the period of charging coupled-inductor in a switching cycle T_S (T_S=1/f_S, f_S is the switching frequency). Secondly, the half-bridge DC-link circuit is composed of switches S_A, S_B, half-bridge capacitor C_{O1}, C_{O2}, and filter capacitor C_L in aim for the DC-AC conversion to supply the load R_L, where C_{O1}, C_{O2} are assumed with the same capacitance (C_{O1}=C_{O2}=C_O). With the help of S_A and S_B in the half-bridge, the maximum range of the AC output V_{OUT} can reach: +0.5[4(n+1)+(1+nD)/(1-D)]V_S~ -0.5[4(n+1)+(1+nD)/(1-D)]V_S. Fig. 2 shows the theoretical waveforms within an output cycle T_O (T_O=1/f_O, f_O is the output frequency). Here, for the convenience of explanation, an output cycle T_O contains 11 (or above actually) switching cycle T_S. Each T_S has two phase: Phase I and II with the different periods DT_S and (1-D)T_S. The detailed operations are discussed as follows.

1) Phase I:

During this time interval, turn on S_0, S_4 and turn off S_1, S_2, S_3. Then, the diodes D_1, D_3-D_9 are turned on, and D_2 is off. The inductor L_1 is charged by supply V_S, and simultaneously the energy is transferred from the first side of the coupled-inductor to the secondary side, then the voltage of V_{L1}=+V_S, V_{L2}=–nV_S. The pumping capacitors C_1-C_4 are charged in parallel by supply V_S together with V_{L2} so as to make V_{C1}, V_{C2}, V_{C3}, V_{C4} reaching the value of (n+1)V_S. At the same time, C_{O1} or C_{O2} is operating as follows. While S_A is ON, the relevant topology is shown in Fig. 3(a). C_{O1} is discharged to supply the energy to C_L and R_L towards the positive output. While S_B is ON, the relevant topology is shown in Fig. 3(b). C_{O2} is discharged to supply the energy to C_L and R_L, towards the negative output.

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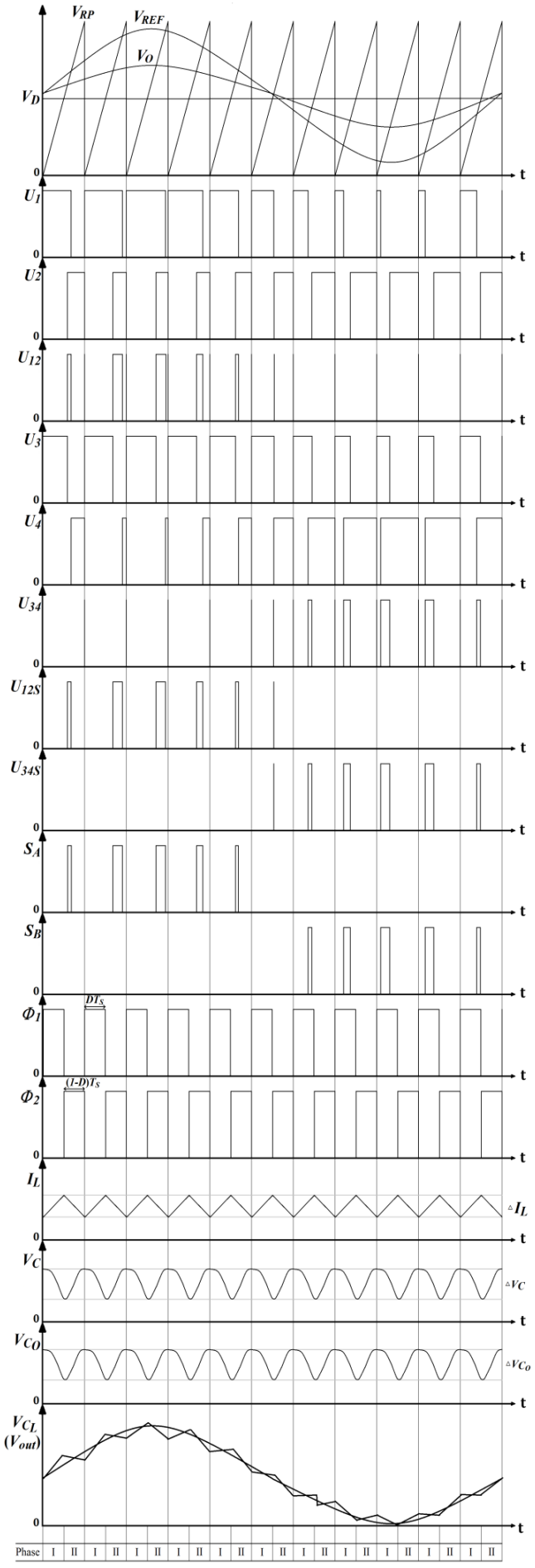

Fig. 2. Theoretical waveforms of SPSCCI Inverter.

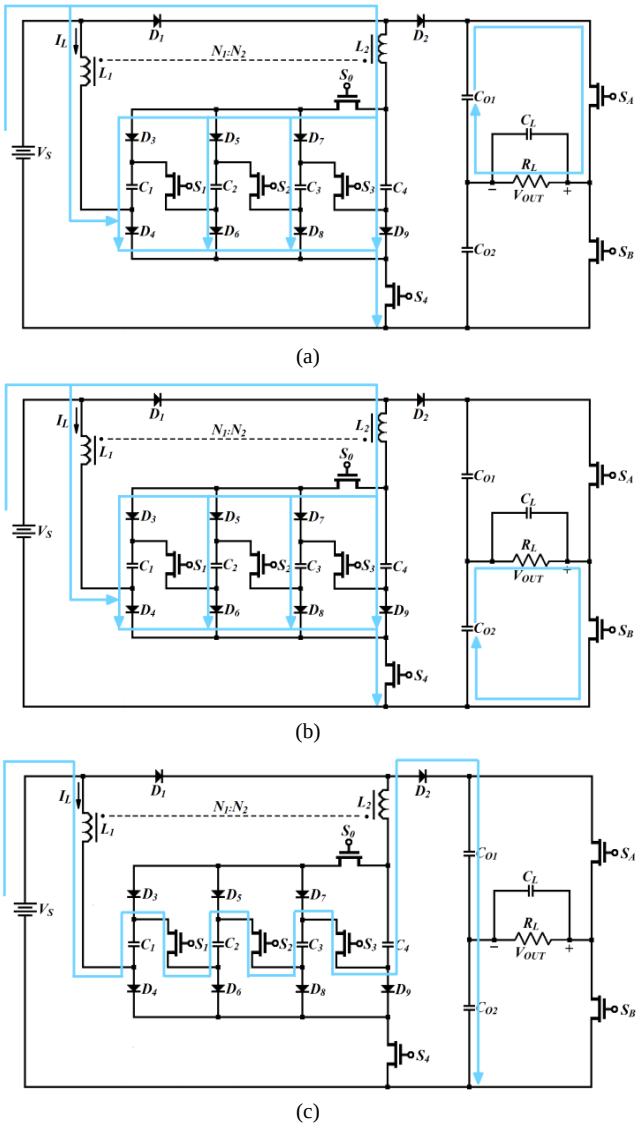

Fig. 3. Topologies for Phase (a) I (S_A:ON), (b) I (S_B:ON), and (b) II.

2) Phase II:

During this time interval, turn on S_1, S_2, S_3, and turn off S_0, S_4. Then, the diodes D_1, D_3-D_9 are turned off, and D_2 is on. The relevant topology is shown in Fig. 3(c). According to the theory of the booster, the steady-state voltage V_{L1} across L_1 is going towards the value of $-DV_S/(1\text{-}D)$ via the operation of duty cycle D, and thus the voltage V_{L2} across L_2 in the secondary side is approaching the value of $+nDV_S/(1\text{-}D)$. Based on the current path as in Fig. 3(c), the half-bridge total capacitor voltage ($V_{CO1}+V_{CO2}$) can be charged by V_S, V_{L1}, V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{L2} in series connection (i.e. $V_S+V_{L1}+V_{C1}+V_{C2}+V_{C3}+V_{C4}+V_{L2}\rightarrow V_{CO1}+V_{CO2}$). Hence, the steady-state voltage of $V_{CO1}+V_{CO2}$ will be boosted into $[4(n+1)+(1+nD)/(1\text{-}D)]V_S$.

Based on the cyclical operations of Phase I and II, the overall step-up gain can reach the value of $[4(n+1)+(1+nD)/(1\text{-}D)]$ theoretically (from V_S to half-bridge total capacitor voltage). Extending the capacitor count, the gain can be $[m(n+1)+(1+nD)/(1\text{-}D)]$, where m is the number of pumping capacitors. Further, with the help of the half-bridge DC-link, the AC output can be realized for the range of $+0.5[m(n+1)+(1+nD)/(1\text{-}D)]V_S \sim -0.5[m(n+1)+(1+nD)/(1\text{-}D)]V_S$.

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B. *Control Part*

The control part of SPSCCI inverter is composed of a two-phase generator and a SPWM controller as in the lower half of Fig. 1. The operations of these two blocks are discussed as follows. Firstly, an adjustable voltage V_D is compared with a ramp function V_{RP} to produce a non-symmetrical clock signal U_0. And then, this clock is sent to the non-overlapping circuit so as to obtain a set of phase signals Φ_1 and Φ_2 for the driver signals of and S_0, S_4 and S_1-S_3. Thus, D is exactly the on-time ratio (duty cycle) of S_0, S_4, and DT_S (period of Phase I) can be regulated by the value of V_D. The main goal is to generate the driver signals of switches for the different topologies.

Secondly, from the controller signal flow, the output voltage V_{OUT} is attenuated and fed back into the OP-amp low-pass filter (LPF) for high-frequency noise rejection. Next, by using a further DC-shift of V_C, V_O is obtained and compared with the desired output V_{REF} via 4 comparators U_1, U_2, U_3 and U_4, and following by using logic-AND to produce a set of control signals U_{12}, U_{34} for realizing SPWM. When e>0 and |e| is raising (e=V_{REF} -V_O), the pulse width of U_{12} is getting bigger. When e<0 and |e| is raising, the pulse width of U_{34} is getting bigger. And then, via the interlock circuit (avoid S_A and S_B being 1 simultaneously) plus coming into the phase of Φ_2, S_A and S_B can be obtained for the SPWM control. The main goal is to keep V_O on following V_{REF} (sinusoidal reference) to enhance the regulation capability of this proposed inverter. To summarize, based on V_O and V_{REF}, the relevant rules of producing the control/driver signals are listed as below.

1) Φ_1, Φ_2: non-overlapping anti-phase signals from U_0;
   S_0=Φ_1; S_4=Φ_1;
   S_1=Φ_2; S_2=Φ_2; S_3=Φ_2;
2) If V_D>V_{RP}, then U_0=1; If V_D<V_{RP}, then U_0=0.
3) If V_{REF}>V_{RP}, then U_1=1; If V_{REF}<V_{RP}, then U_1=0;
   If V_{RP} >V_O, then U_2=1; If V_{RP}<V_O, then U_2=0;
   If V_O >V_{RP}, then U_3=1; If V_O<V_{RP}, then U_3=0;
   If V_{REF}>V_{RP}, then U_4=1; If V_{REF}<V_{RP}, then U_4=0;
4) If U_1=1 and U_2=1, then U_{12}=1 (otherwise U_{12}=0);
   If U_3=1 and U_4=1, then U_{34}=1 (otherwise U_{34}=0);
5) If U_{12}=1 and Φ_2=1, then U_{12S}=1 (else U_{12S}=0);
   If U_{34}=1 and Φ_2=1, then U_{34S}=1 (else U_{34S}=0);
6) SPWM control signals: (^: logic-AND)
   S_A= U_{12S} ^Φ_2, for V_{REF} >V_O;
   S_B= U_{34S} ^Φ_2, for V_{REF}<V_O.

III. Examples of SPSCCI Inverter

In this paper, the proposed SPSCCI is simulated by SPICE, and all the parameters are listed in TABLE I. There are totally 3 cases for steady-state responses and 4 cases for dynamic responses respectively. Then, these results are illustrated to verify the efficacy of the proposed inverter.

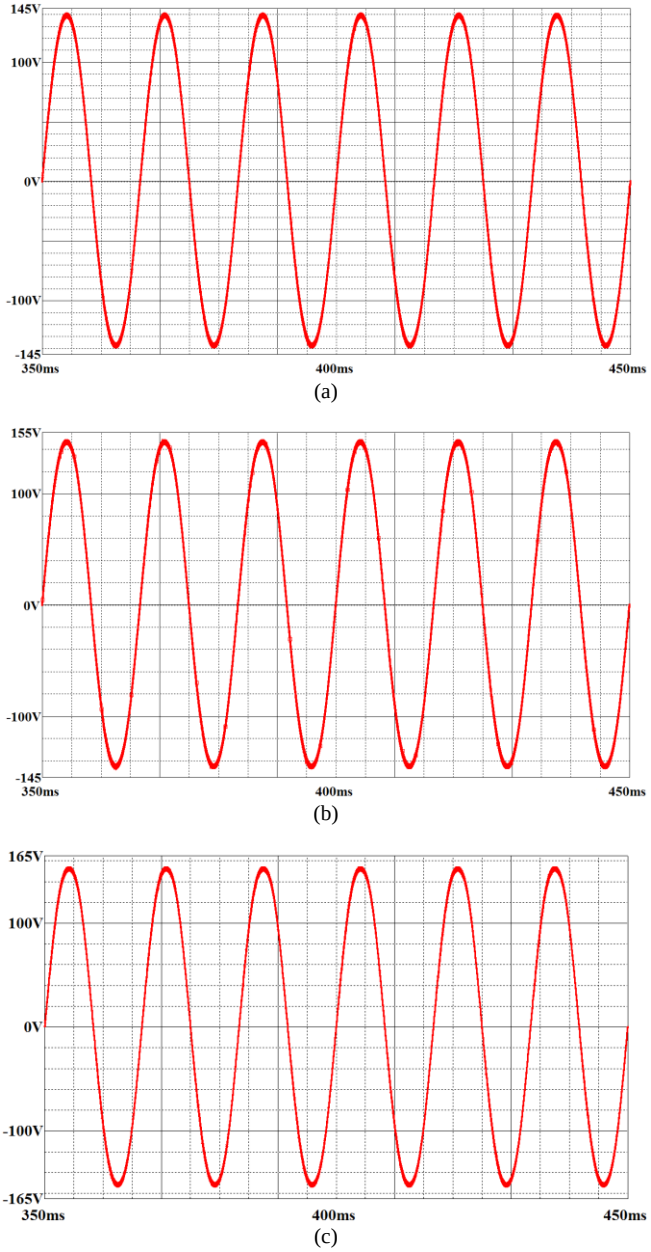

Fig. 4. Output V_{OUT} for V_{REF}: (a) f_O =60Hz, V_m =145V; (b) f_O=60Hz, V_m=155V; (c) f_O =60Hz, V_m=165V.

1) Steady-State Responses:

Case 1: f_O=60 Hz, V_m=145V

Let the supply source V_S be DC 12V, load R_L be 700Ω, and the peak value and output frequency of V_{REF} are V_m=145V, f_O=60Hz. The waveform of V_{OUT} is obtained as in Fig. 4(a). V_{OUT} has the practical peak value of 141V (i.e. 99.7V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 67.3% and THD is 2.298%.

Case 2: f_o=60 Hz, V_m=155V

Let the supply source V_S be DC 12V, load R_L be 700Ω, and the peak value and output frequency of V_{REF} are V_m=155V, f_O=60Hz. The waveform of V_{OUT} is obtained as in Fig. 4(b). V_{OUT} has the practical peak value of 148V (i.e. 104.7V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 70.1% and THD is 2.693%.

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Case 3: f_O=60 Hz, V_m=165V

Let the supply source V_S be DC 12V, load R_L be 700Ω, and the peak value and output frequency of V_{REF} are V_m=165V, f_O=60Hz. The waveform of V_{OUT} is obtained as in Fig. 4(c). V_{OUT} has the practical peak value of 158V (i.e. 111.7V_{RMS}), and the practical output frequency is about 60Hz. The efficiency is 71.3% and THD is 3.799%.

2) Dynamic Responses:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a variation of source voltage V_S must be considered, as well as variation of load R_L and/or reference V_{REF} (f_O or V_m).

Case 1: V_S variation

Assume that V_S is normally at DC 12V, and then it has an instant voltage jump of 12V→11V on 400ms (V_{REF} : f_O=60Hz, V_m=145V). The waveform of V_{OUT} is shown as in Fig. 5(a). Obviously, V_{OUT} has a slight decrease into about 138V.

Case 2: R_L variation

Assume that R_L is 1kΩ normally, and it suddenly changes from 1kΩ to 0.5kΩ on 400ms (V_{REF} : f_O= 60Hz, V_m=145V). Fig. 5(b) shows the transient waveform of V_{OUT} at the moment of loading variation. Obviously, V_{OUT} has a small drop but can still be following V_{REF}.

Case 3: f_O variation

Assume that the frequency f_O of V_{REF} is 60Hz normally. After a period of 400ms, and it suddenly changes from 60Hz to 120Hz. Fig. 5(c) shows the transient waveform of V_{OUT} at the moment of variation: f_O =60Hz→120Hz (V_m=165V). Obviously, V_{OUT} is still able to follow V_{REF} even the frequency of V_{REF} changes.

Case 4: V_m variation

Assume that V_m is 165V normally, After a period of 400ms, and it changes from 165V to 145V. Fig. 5(d) shows the transient waveform of V_{OUT} at the moment of variation: V_m=165V→145V. Obviously, V_{OUT} is still able to follow V_{REF} even the amplitude of the desired V_{REF} changes.

According to the above results, it is obvious that V_{OUT} is following V_{REF} for the cases, including V_S source variation, R_L loading variation, f_O frequency variation, V_m amplitude variation. These results show that this proposed inverter has a good closed-loop dynamic performance.

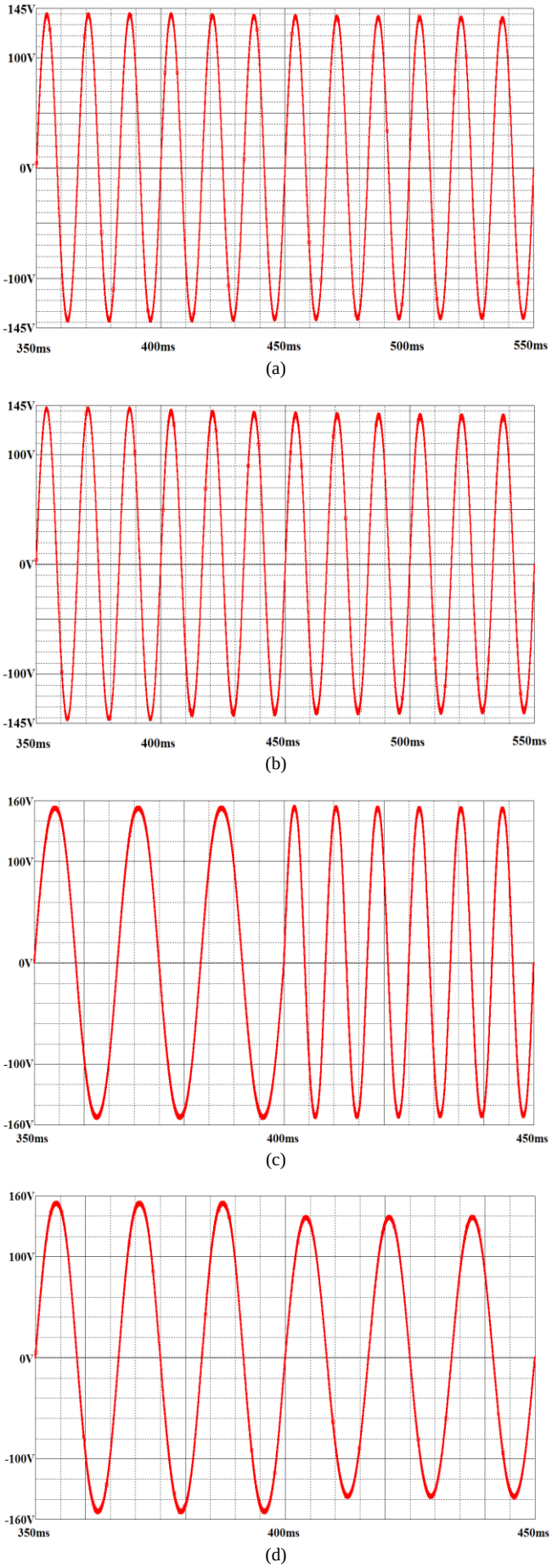

Fig. 5. Output V_{OUT} for the variation of (a) V_S; (b) R_L; (c) f_O; (d) V_m.

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TABLE I
Circuit parameters of SPSCCI inverter.

Supply source (V_S)	12V
Pumping capacitor (C_1-C_4)	22μF
Coupled-inductor(L_1, L_2)	40μH, 640μH (n=4)
Half-bridge capacitor (C_{O1}, C_{O2})	80μF
Output capacitor (C_L)	1.2μF
Power MOSFETs (S_0-S_5, S_A, S_B)	ASW
On-state resistor of MOSFETs (S_0-S_5)	50μΩ
On-state resistor of MOSFETs (S_A, S_B)	2.2Ω
Diode (D_1-D_9)	D1N5822
Load resistor (R_L)	700Ω
Switching frequency (f_S)	50kHz
Output frequency (f_O)	60Hz

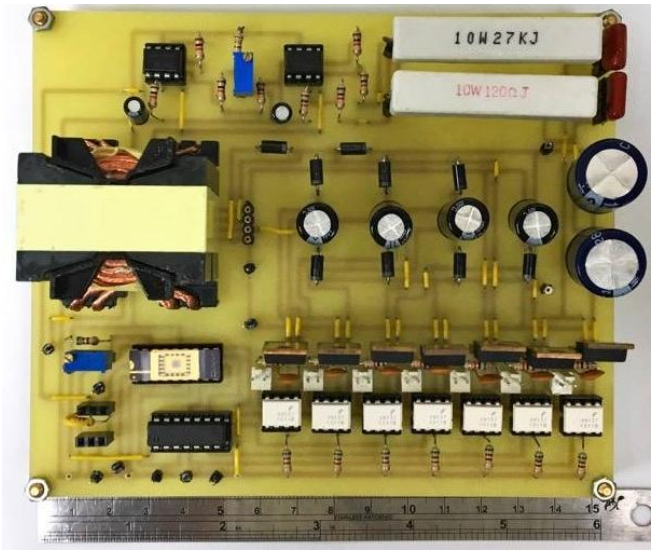

Fig. 6. Prototype circuit of SPSCCI inverter.

IV. Conclusion

A closed-loop scheme of a high-gain SPSCCI boost DC-AC inverter is proposed by combining a two-phase generator and SPWM controller for low-power step-up DC-AC conversion and regulation (SPSCCI: DC $V_S \rightarrow$ AC V_{OUT}: $+0.5[m(n+1)+(1+nD)/(1-D)]V_S \sim -0.5[m(n+1)+(1+nD)/(1-D)]V_S$). Finally, the closed-loop SPSCCI inverter is designed and simulated by SPICE for some cases: steady-state and dynamic responses. The advantages of the proposed scheme are listed as follows. (i) This SPSCCI needs just one coupled-inductor element (inductor). Except this, other components (i.e. SC) will be able to be made in IC fabrication future. (ii) This proposed inverter can provide a high voltage gain (from V_S to half-bridge total capacitor voltage) of $[4(n+1)+(1+nD)/(1-D)]$ at most. (iii) For a higher gain, it can be realized with increasing the turn ratio of coupled-inductor or extending the number of pumping capacitors. (iv) The SPWM technique is adopted not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading variation. At present, the prototype circuit of this inverter is implemented in the laboratory as shown in the photo of Fig. 6. Some experimental results will be obtained and measured for the verification of the proposed inverter.

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