# A High-Gain Cockcroft-Walton-Doubler-Based Switched-Coupled-Inductor Step-Up DC-DC Converter

Yuen-Haw Chang and Yu-Ming Lu

***Abstract*—A closed-loop high-gain Cockcroft-Walton-doubler-based switched-coupled-inductor (CWSCI) converter is proposed by combining a sawtooth wave generator and pulse-width- modulation-based (PWM-based) compensator for step-up DC-DC conversion and regulation. The power part between source $V_S$ and output $V_O$ contains two sub-circuits: (i) a switched-coupled- inductor (SCI) booster, and (ii) a two-stage Cockcroft-Walton- doubler (CWD) circuit. With the help of these circuits operating cyclically, this CWSCI can provide the total step-up voltage gain of $(2n+3+nD)/(1-D)$ theoretically, where $D$ is the duty cycle of PWM and $n$ is the turn ratio of the coupled inductor (e.g. the voltage gain can be boosted up to 21 when $D$=0.5, $n$=3). Further, the PWM technique is adopted not only to enhance the output regulation for the compensation of the dynamic error between the practical and desired outputs, but also to reinforce the robustness against source/loading variation. Finally, the closed-loop CWSCI is designed by OrCAD and simulated for some cases: steady-state and dynamic responses. All results are illustrated to show the efficacy of the proposed scheme.**

***Index Terms*—high-gain, Cockcroft-Walton-doubler (CWD), switched-coupled-inductor (SCI), step-up DC-DC converter, pulse-width-modulation (PWM).**

## I. Introduction

With the rapid development of power electronics, the step-up DC-DC converters are emphasized more widely for electricity-supply applications, such as photo-voltaic system, fuel cell, X-ray systems. In general, these power electronics converters are always required for a high efficiency, a small volume, a light weight, and a strong regulation capability.

The switched-capacitor converter (SCC), possessed of the charge pump structure, is one of solutions to DC-DC power conversion because it has only semiconductor switches and capacitors. Unlike traditional converters, the inductor-less SCC has light weight and small volume. Up to now, many types have been suggested [1]-[2], and some well-known topologies are presented, e.g. Dickson charge pump, Ioinovici SC. In 1976, Dickson charge pump was proposed with a two-phase diode-capacitor chain [3]-[4], but it has the drawbacks of fixed gain and large device area. In the 1990s, Ioinovici proposed a SCC with two sym-metrical capacitor cells, and presented a current-mode SCC [5]-[6]. In 1997, Zhu and Ioinovici performed a com-prehensive steady-state analysis of SCC [7]. In 1998, Mak and Ioinovici suggested a high-power-density SC inverter [8]. In 2004, Chang presented a current-mode SC inverter [9]. In 2009, Tan *et al.* proposed the modeling and design of SCC by variable structure control [10]. In 2011, Chang proposed an integrated step-up/down SCC (SCVM/SCVD) [11]. In 2013, Chang proposed a gain/efficiency-improved serial-parallel switched-capacitor converter (SPSCC) by combining an adaptive-conversion-ratio (ACR) and PWM control [12]. In 2014, Chang proposed a high-gain scheme of switched-inductor switched-capacitor step-up DC-DC converter (SISCC) [13]. In 2015, Wu proposed a non-isolated high step-up DC-DC converter adopting switched-capacitor cell [14].

In order to increase the voltage gain, it is one of the good ways to utilize the device of coupled-inductor. However, the stress on transistors and the volume of magnetic device might be considered. In 2011, Berkovich *et al.* proposed a switched-coupled-inductor cell for DC-DC converter with very large conversion ratio [15]. In 2015, Chen *et al.* proposed a novel switched-coupled-inductor DC-DC step-up converter via adopting a coupled inductor to charge a switched capacitor for making voltage gain effectively increased [16]. Not only lower conduction losses but also higher power conversion efficiency is benefited from fewer device count. For achieving a compromise among volume size, device count, and voltage gain, the closed-loop CWSCI is proposed by referring to the ideas of [11]-[18] for the high-gain DC-DC conversion and regulation.

## II. Configuration of CWSCI

Fig. 1 shows the overall configuration of Cockcroft-Walton-doubler-based switched-coupled-inductor (CWSCI) step-up DC-DC converter, and it contians two major parts: power part and control part for achieving the high-gain DC-DC conversion and closed-loop regulation. The details of these two parts are discussed as follows.

### *A. Power Part*

The power part of CWSCI is shown in the upper half of Fig. 1 and it consists of two sub-circuits: a switched-coupled-inductor booster (SCI booster) and a two-stage Cockcroft-Walton doubler (CWD), connected in cascade between source $V_S$ and output $V_O$. This converter contains one coupled inductor ($L_1$, $L_2$) with the turn ratio $n=N_2/N_1$, one power switch ($S_1$), four pumping capacitors ($C_1$-$C_4$) of two-stage CWD, one output capacitor $C_o$, and five diodes

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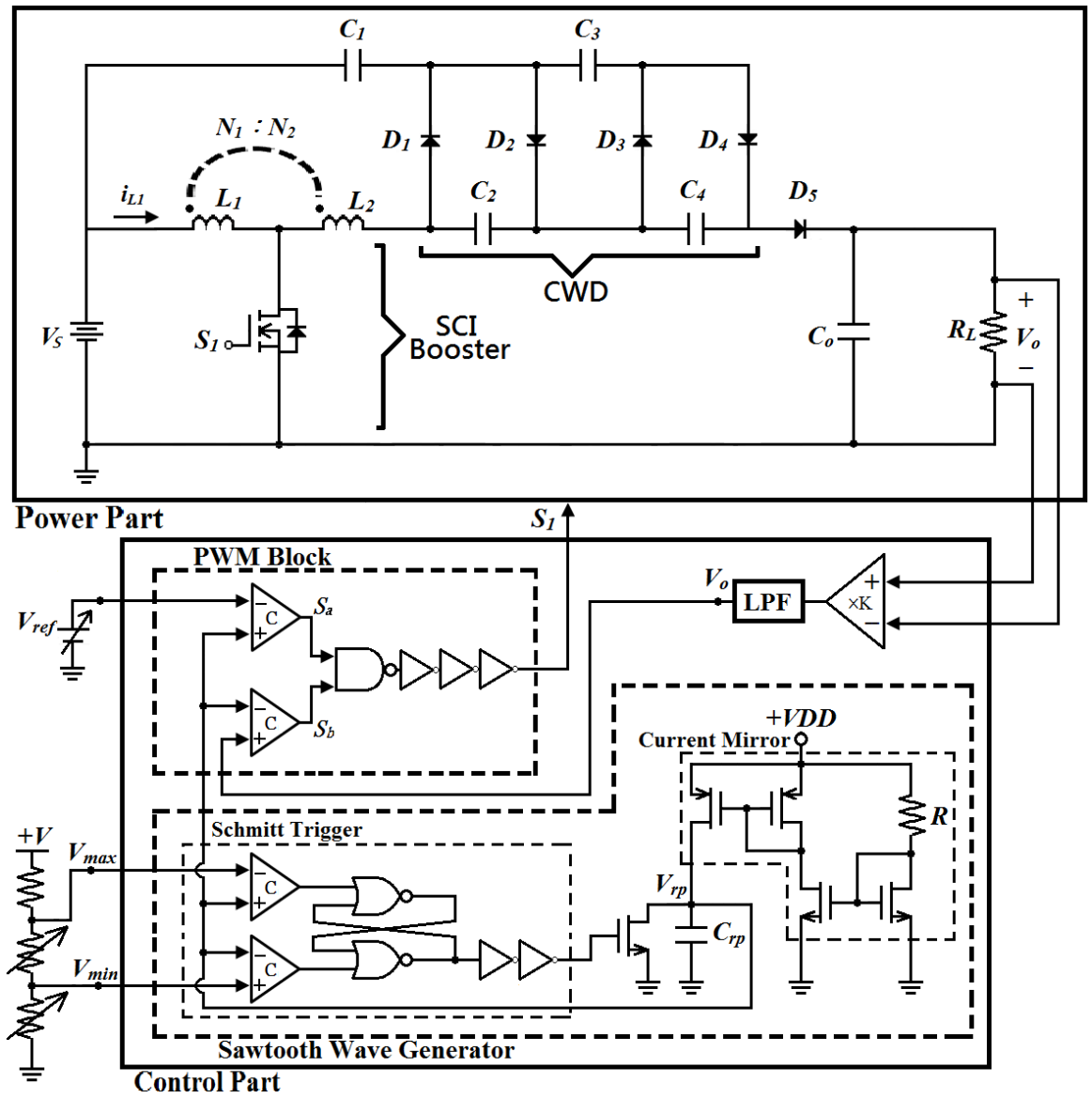


Fig. 1. Closed-loop configuration of CWSCI.

($D_1$-$D_5$), where each capacitor in CWD has the same capacitance $C$ ($C_1$=$C_2$=$C_3$=$C_4$=$C$). Fig. 2 shows the theoretical waveforms of CWSCI in a switching cycle $T_S$ ($T_S$= $1/f_S$, $f_S$: switching frequency). Each $T_S$ includes two phases: Phase I (phase duration: $DT_S$) and Phase II (phase duration: $(1\text{-}D)T_S$), where $D$ ($0<D<1$) is the duty cycle of PWM. The operations for Phase I and II are described as follows.

(i) Phase I:

During the period of Phase I, $S_1$ is turned ON. Then, the diodes $D_2$ and $D_4$ are turned ON, and $D_1$, $D_3$ are OFF. The current-flow path is shown as "---" in Fig. 3(a). The inductor $L_1$ is charged by source $V_S$, and the energy is simultaneously transferred from the primary side of the coupled inductor into the secondary side for making the voltage across $L_2$ being $nV_S$. Then, the capacitors $C_2$, $C_4$ are charged by $V_S$ in series together with $L_2$, $C_1$ and $C_3$. At the same time, output capacitor $C_o$ just stands alone to supply load $R_L$.

(ii) Phase II:

During the period of Phase II, $S_1$ is turned OFF. Then, the diodes $D_1$ and $D_3$ are turned ON, and $D_2$, $D_4$ are OFF. The current-flow path is shown as --- in Fig. 3(b). $L_1$, $L_2$, $C_2$ and $C_4$ are dicharged in series together with $V_S$ to transfer the energy to output capacitor $C_o$ and load $R_L$. At the same time, the capacitors $C_1$ and $C_3$ are charged by the series voltages of inductors $L_1$, $L_2$ and $C_2$.

Based on the scheduled operations of Phase I and Phase II cyclically, the overall step-up gain can reach the value of $[1+nD+2(n+1)]/(1\text{-}D)=(2n+3+nD)/(1\text{-}D)$ theoretically ($V_S+|V_{L1}|+|V_{L2}|+|V_{C2}|+|V_{C4}| \rightarrow V_O$). Via extending the capacitor count, the gain can reach up to $[1+nD+m(n+1)]/(1\text{-}D)$, where $m$ is the stage number of CWD.

## B. Control Part

The control part of CWSCI is shown in the lower half of Fig. 1. It is composed of a sawtooth wave generator and PWM block. In the sawtooth wave generator, a current mirror is employed for generating a constant current source to charge the capacitor $C_{rp}$, and then voltage $V_{rp}$ across this $C_{rp}$ is linearly increasing like a ramp. Next, $V_{rp}$ is sent and

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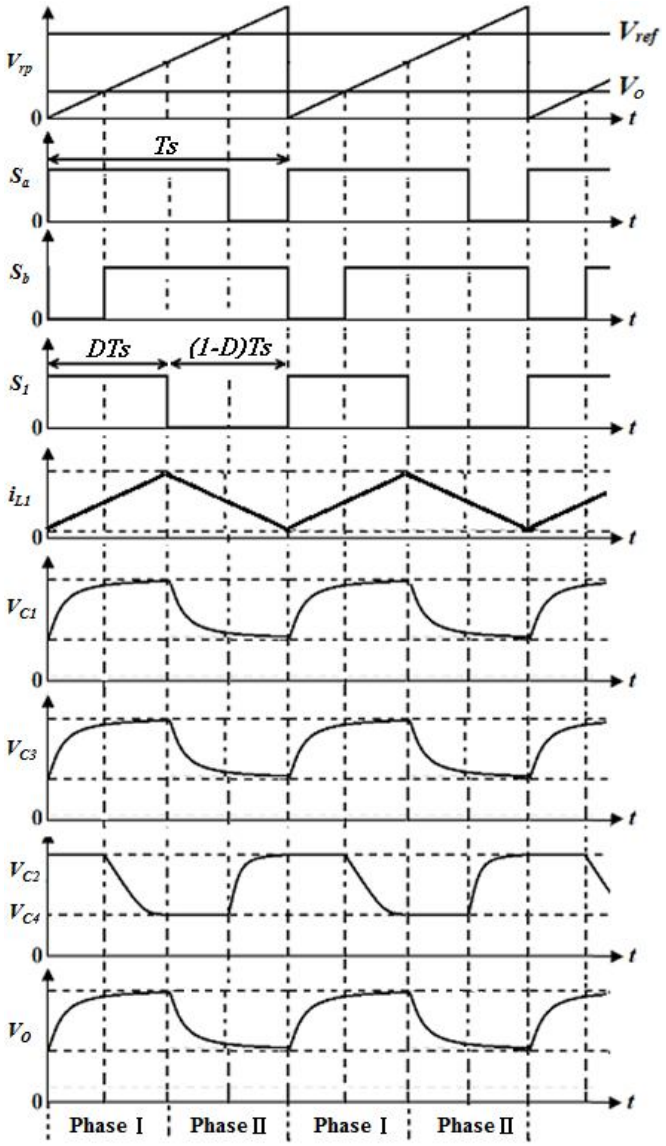


Fig. 2. Theoretical waveforms of CWSCI.

compared with two external voltages $V_{max}$ and $V_{min}$ in the Schmitt trigger in order to keep $V_{rp}$ being in the range between $V_{max}$ and $V_{min}$, just like the waveforms as in Fig. 2. From the controller signal flow, the feedback signal $V_O$ is sent into the OP-amp low-pass filter (LPF) for high-frequency noise rejection. The filtered signal $V_O$ is compared with the desired output reference $V_{ref}$ to produce the driver signal of switch $S_1$ via the PWM block ($D$ is the duty cycle of PWM for $S_1$). The goal of PWM control is to keep $V_O$ on following the different desired $V_{ref}$ for the better output regulation. If $V_S$ or $R_L$ is suddenly decreasing (source/loading variation), $V_O$ will be going down. The error between $V_{ref}$ and $V_O$ is rising quickly. The bigger error makes a larger duty cycle $D$ via PWM, and then this $D$ will drive $V_O$ to follow $V_{ref}$. In this paper, the closed-loop control will be achieved via the PWM-based compensator to improve the regulation capability of this converter.

## III. EXAMPLES OF CWSCI

In this section, based on Fig. 1, this closed-loop converter is designed and simulated by OrCAD SPICE tool. The results are illustrated to verify the efficacy of the proposed converter. The component parameters of the

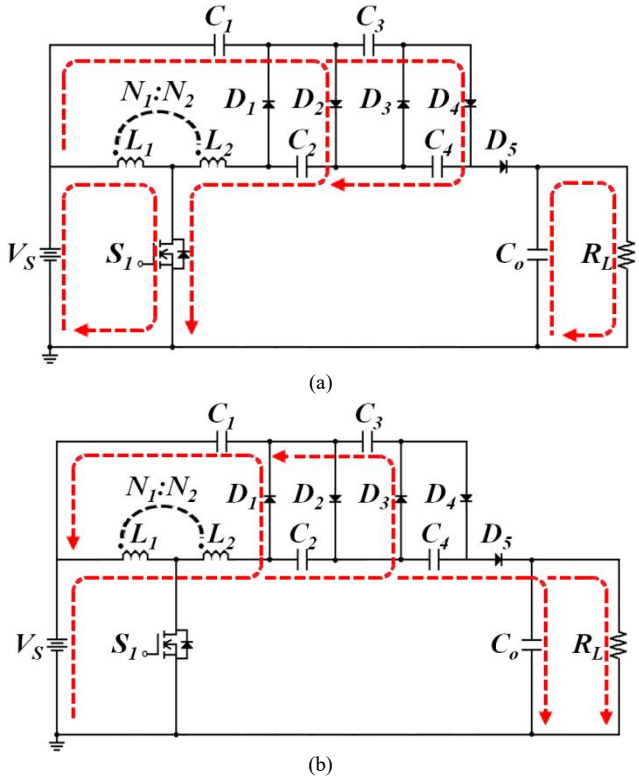


Fig. 3. Topologies for Phase (a)I, and (b)II.

Table I. Component parameters of CWSCI.

| | |
|---|---|
| Supply source ($V_S$) | 24V |
| Pumping capacitor ($C_1$~$C_4$) | 47uF |
| Output capacitor ($C_O$) | 180uF |
| Inductor ($L_1$, $L_2$) | $L_1$=100uH, $L_2$=900uH ($n$=3) |
| Switching frequency ($f_S$) | 50kHz |
| Diodes : $D_1$~$D_5$ | D1N5820 |
| On-state resistance of switch | 50uΩ |
| Load resistor ($R_L$) | 5kΩ |

CWSCI are listed in Table I. This converter is preparing for supplying the load $R_L$=5kΩ. For closed-loop performances, some topics will be simulated and discussed, including: (i) steady-state responses, and (ii) dynamic responses.

(i) Steady-state responses:

The closed-loop CWSCI is simulated for $V_{ref}$ = 504V / 480V / 460V respectively, and then these output results are obtained as shown in Fig. 4(a)-(b) / 4(c)-(d) / 4(e)-(f). In Fig. 4(a), it can be found that the settling time is about 40ms, and the steady-state value of $V_O$ is really reaching 503.96V. This converter is stable to keep $V_O$ following $V_{ref}$ (504V). In Fig. 4(b), the output ripple percentage (rp) is measured as rp = $\Delta v_o/V_O$ = 0.0012%, and the power efficiency is obtained as $\eta$= 95.60%. In Fig. 4(c), the settling time is about 40ms, and the steady-state value of $V_O$ is really reaching 478.90V. In Fig. 4(d), the output ripple percentage is measured as rp = $\Delta v_o/V_O$ = 0.0010%, and the power efficiency is obtained as $\eta$= 95.31%. In Fig. 4(e), the settling time is about 40ms, and the steady-state value of $V_O$ is really reaching 458.68V. In Fig. 4(f), the output ripple percentage is measured as rp = $\Delta v_o/V_O$ = 0.0008%, and the power efficiency is obtained as $\eta$= 91.52%. These results show that this converter has a high voltage gain and a good steady-state performance.

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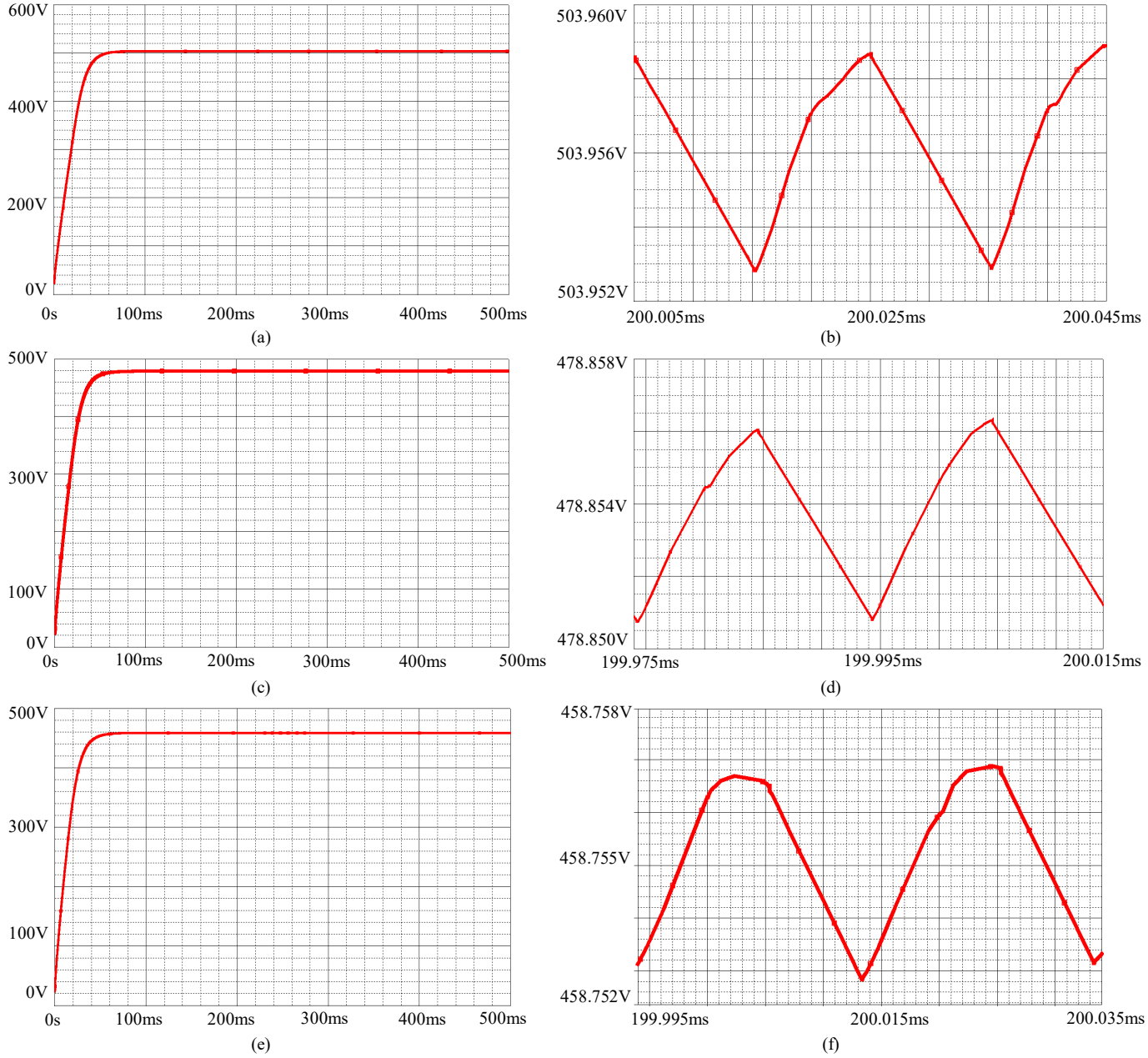


Fig. 4. Steady-state responses of CWSCI.
(a)$V_O$ for $V_{ref}$=504V, (b) rp=0.0012%; (c) $V_O$ for $V_{ref}$=480V, (d) rp=0.0010%; (e) $V_O$ for $V_{ref}$=460V, (f) rp=0.0008%.

(ii) Dynamic responses:

Since the voltage of battery is getting low as the battery is working long time, or the bad quality of battery results in the impurity of source voltage, such a voltage variation should be considered as well as loading variation.

(a) Case I: (source variation)

Assume that $V_S$ is the DC value of 23.5V and extra plus a sinusoidal signal disturbance of 1$V_{P\text{-}P}$ as in Fig. 5(a), and then the waveform of $V_O$ is obtained in Fig. 5(b) ($V_{ref}$=490V). Clearly, by using the closed-loop control, $V_O$ is still keeping on $V_{ref}$ in spite of source disturbance.

(b) Case II: (loading variation)

Assume that $R_L$ is 5kΩ normally, and it changes from 5kΩ to 2.5kΩ. After a short period of 300ms, the load recovers from 2.5kΩ to 5kΩ, i.e. $R_L$=5kΩ→2.5kΩ→5kΩ as in Fig. 5(c) ($V_{ref}$=490V). Fig. 5(d) shows the transient waveform of $V_O$ at the moment of loading variation. It is found that $V_O$ has a small drop (5V, i.e. 5V/490V=1.02%) at $R_L$: 5kΩ→2.5kΩ (double loading). Of course, the curve becomes thicker during the heavier load, i.e. the ripple becomes bigger at this moment.

(c) Case III: (reference variation)

Assume that $V_{ref}$ is 504V normally, and it suddenly changes from 504V to 480V. After a short period of 400ms, the $V_{ref}$ recovers from 480V to 504V, i.e. $V_{ref}$=504V→480V→504V as in Fig. 5(e). The waveform of $V_O$ is obtained in the Fig. 5(f). It is found that $V_O$ is still following $V_{ref}$ via the closed-loop compensation, even though $V_{ref}$ has a change of 24V.

These results show that the closed-loop CWSCI has the good output regulation capability to source/loading variation as well as reference variation.

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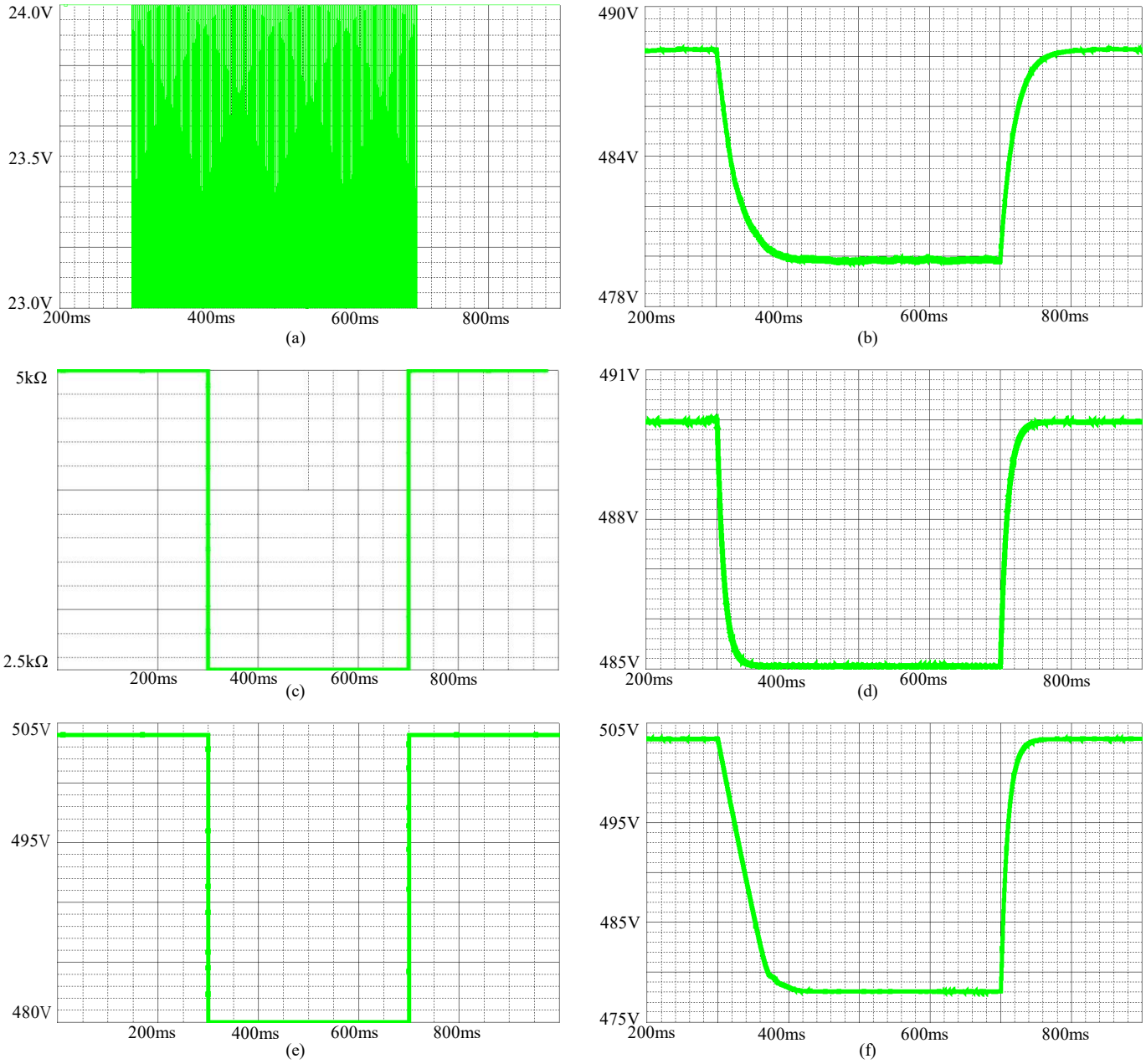


Fig. 5. Dynamic responses of CWSCI.
(a)$V_S$=23.5+sin(2π×1000t) V (b) $V_O$ (Case Ⅰ); (c) $R_L$=5kΩ→2.5kΩ→5kΩ, (d) $V_O$ (Case Ⅱ); (e) $V_{ref}$=504V→480V→504V, (f) $V_O$ (Case Ⅲ).

## IV. Conclusions

A closed-loop high-gain CWSCI converter is proposed by combining a sawtooth wave generator and PWM-based compensator circuit for step-up DC-DC conversion and regulation. The advantages of the proposed scheme are listed as follows. (i) In the CWSCI, the large conversion ratio can be achieved with one switch, one coupled inductor, and four capacitors for a step-up gain of 21 or above. (ii) As for the higher step-up gain, it is easily realized through increasing the turn ratio or extending the stage number of CWD. (iii) The PWM technique is adopted here not only to enhance output regulation capability for the different desired output, but also to reinforce the output robustness against source/loading/reference variation. At present, the prototype circuit of CWSCI is implemented in the lab as the photo in Fig. 6. The relevant experiments will go on for measurement and verification of the proposed converter.

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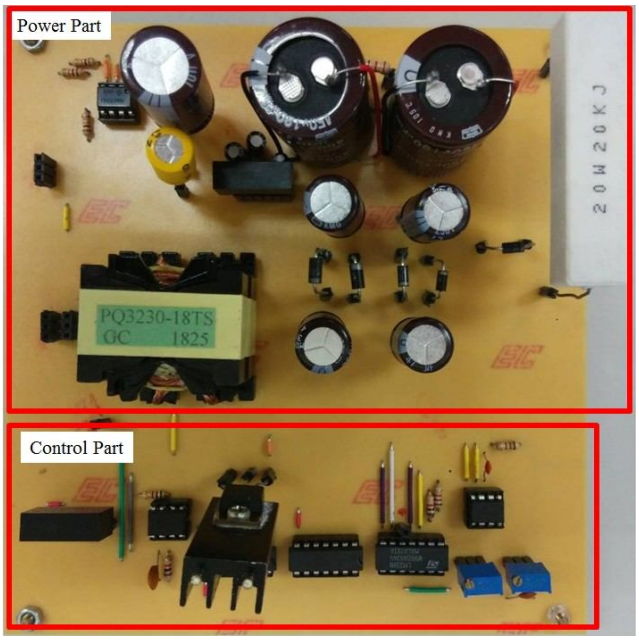


Fig. 6. Prototype circuit of CWSCI.

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