

Key Power Measurements and their Automation in Post Silicon Validation

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Abstract—Power consumed by a chip has become a matter of keen concern in most of the chip design. In today's automotive world, there is a rising need to design chips, which consume minimal power. In such a scenario, it is critical to make a very good plan of all the key power measurements that have to be taken as part of post-silicon validation for analysis of the power consumed by the chip. Also these measurements have to be made at various operating conditions with changes in various parameters. These results will have to be made available across, in a very readable format. Due to higher number of chip derivatives per year and increased set of measurements, this activity consumes a predominant amount of time. In order to achieve reliable and repeatable results within a short period of time and to reduce the manual effort, automation of these measurements could be of great help.

In this paper, we report a methodology in taking right power measurements and also in automating these measurements which reduces the effort in terms of both man power and time, in such a way that the results are produced as early as possible for any kind of analysis.

Index Terms— automation, measurements, post-silicon, power, pre-silicon, Validation.

I. INTRODUCTION

The space of post-silicon power measurements is very vast, and when the silicon arrives in the lab, there are a lot of measurements that can be taken on the silicon. But which of these measurements are really critical, and which of these measurements will really give us important information, is something we need to ponder about. Also these measurements have to be made available immediately after the silicon arrives in the lab.

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The faster they are made available the better it is for the design/concept community to come to conclusions about their designs. This also helps us guide the customers to use appropriate configurations of the chip, to achieve power efficient systems. In automotive industry, chips are a part of several ECUs, and it is critical to know the power consumed by the entire electronics of the car. To get these results as early as possible, it is best to automate the entire measurement setups. This would help in getting reliable and repeatable results, and also enable us to do comparative study across several chips of the same family.

II. WHAT TO MEASURE

Here was adopted a methodology to study all the measurements that are taken in pre-silicon phase for the modules, and to replicate these measurement in post-silicon. This would help in very easy comparison of the power consumption measurements by the modules in pre-silicon and post-silicon phases. All the IP's which are present in the chip are made active using software. These are referred to as power patterns. It would be good to use the same patterns for pre-silicon and post silicon as these measurements can be easily compared. These patterns can themselves have many flavors. They can be configured to mimic realistic scenarios. They can also be configured to mimic stress scenarios, where all the modules (all their instances) are made to run at a maximum frequency. Using these patterns, we can find the total current that would be consumed by the chip- A (across the different power rails that the chip operate on). On the fly, some of the modules can be disabled, and we can see a dip in the power consumed -B. This delta A-B will give the power consumed by the module itself. In this way, we can find the power consumed by all the modules. While taking these measurements, based on the module, it might also be interesting to find out the power that is consumed by the same module, when it is operated at different frequencies, and when it is operating in different modes. It is also essential to find the power consumed by the chip when it is operating at different bus frequencies. Again these patterns can be configured for different frequencies, and the measurements can be taken. CPU (all CPUs if more than one) currents are another important measurement.

Another set of interesting measurement, is to find the total power consumed by the chip at different temperatures. It can cover the entire operating range of the chip. This would help in leakage current calculations. In all these measurements it is important that at each measurement, only one parameter is varied, so that we know for sure that the increase or the decrease in the current is only due to the change in that parameter and nothing else. So if measurements are made at room temperatures, it would be ideal to maintain the constant temperatures of the chip with equipment like the thermostream.

III. WHY TO AUTOMATE THESE MEASUREMENTS?

From the above mentioned list of measurements, it can be said that it is essential to measure the current consumed by the chip with varying operating voltages, bus frequencies and ambient temperatures. This task will make a validation engineer change various parameters each time, measure the current consumed during that particular change and then save those measurement results. This procedure can be done thoroughly for one particular chip through manual execution. But due to the increase in the customer requirements, there exists multiple numbers of chip derivatives taped out in a short period of time (refer to Fig 1). Hence, current measurements for all these derivatives require a large amount of effort and time of a validation engineer. Here comes the importance of automating these measurements. If the manual measurements taken for one particular chip requires 1-2 weeks of effort and time, the same measurement when automated requires only 40-50% of the total effort and time taken during manual execution. After the measurement, logging the results in a document in a customer specified format for analysis is also an important task, which also can sometimes go wrong due to manual entry. So automation of logging these results also plays an important role.

	JUNE					JULY			
SILICO N	23	24	25	26	27	28	29	30	
Chip 1							VEES-RT		
Chip 2				VEES-RT					
Chip 3	VEES-RT								
Chip 4								ES	
Chip 5								VEES-RT	

VEES - Very Early engineering samples
SPLIT - Split Samples
ES - Engineering Samples

Fig 1: Representation of various chip derivatives coming in each calendar week

IV. ALGORITHM ON TEST EXECUTION USING AUTOMATION

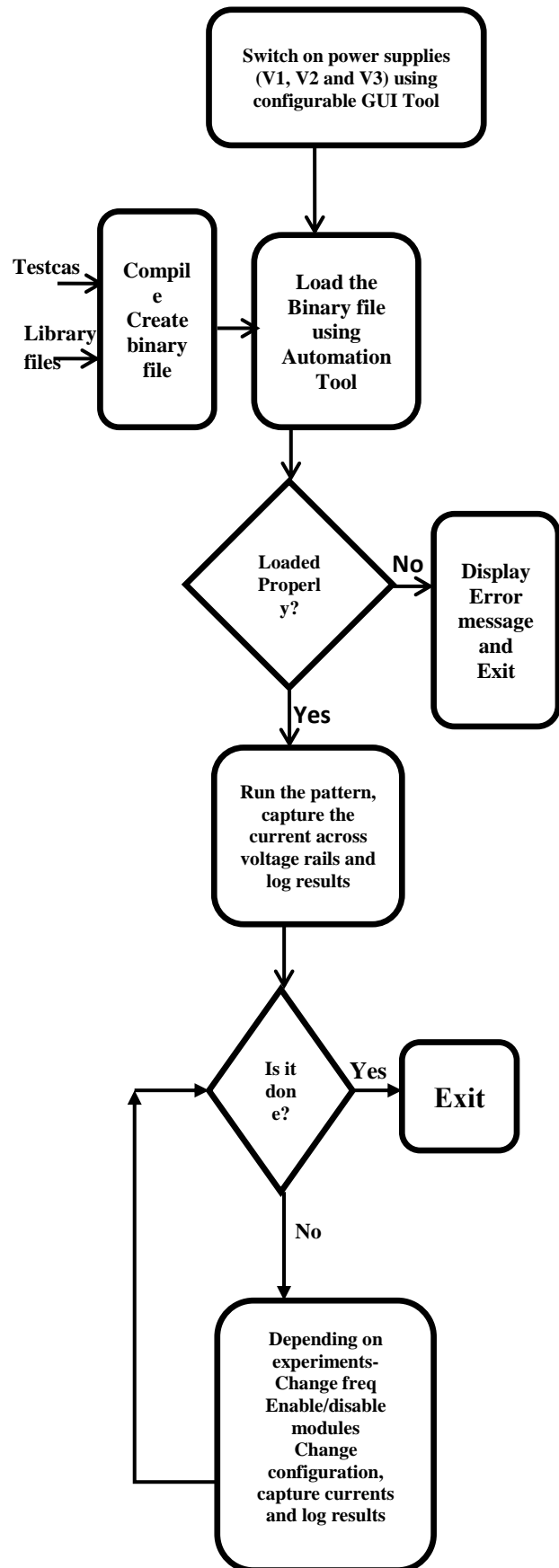


Fig 2: Algorithm on Automation Methodology for Power measurements

V. OUR APPROACH

A configurable GUI is used to simplify the system validation, debug etc. It provides a portable and scalable architecture and with simple configuration and user friendly interface. This interface comes with the perl and python support. So user can code a perl script for loading the binary file of the power pattern into the chip and then executing the pattern. All IP's in the microcontroller starts running in the background. Various bus frequencies are varied by changing the register values and voltages and ambient temperatures are varied through controlling the digital DC Power Supply and thermostream with the help of the script written by the user, which in turn is executed by the GUI. Once the chip reaches a stable state, the current consumed by the chip is measured and logged down into a report, which is generated and saved into the Host PC for the stakeholders to access it easily (Refer to Fig 3). This eliminates hundreds of hours from the total manual measurement time. Also, there exists a standard report each time a measurement is taken.

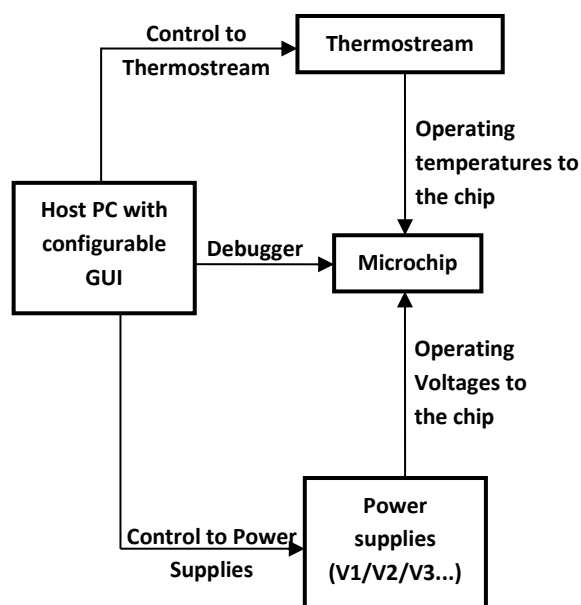


Fig 3: Architecture of Automation methodology

VI. RESULTS

The effort reduction from manual execution to the automation of measurements is depicted in the following chart (Refer Fig 4).

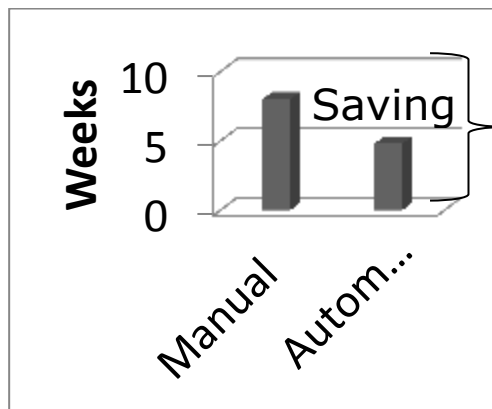


Fig 4: Effort Reduction from Manual to Automation of Measurements

VII. CONCLUSION

The concept and design community is facing multiple conflicts in understanding and targeting the power hungry areas in the modules for next generation chips of same family. These measurements made their understanding on current consumption values easy. Also, with the help of the methodology we used in automating power measurements, various customers could get instant and accurate power estimates of the chip during chip delivery. Along with the customers, it has become easy for an engineer to repeat the measurements on multiple silicons before sharing the reliable results. It saves around 40-50% of effort and time to get the results.

APPENDIX

TABLE I
 CPU MEASUREMENT RESULTS CAPTURED DURING AUTOMATION.

CPU specificSoC	Frequency / Throttling	CPUx	CPUy	CPUz
Real, Ta = 125°C, thermo = 150°C V= +10%, IPC = 0,6				
Max, Ta = 125°C, thermo = 150°C V= +10%, IPC = 1,4				
Here CPUx,y,z are at different frequencies with and without lock step.				

TABLE II
POWER CONSUMPTION MEASUREMENTS AT VARIOUS BUS
FREQUENCIES

F _{Bus1}	F _{Bus2}	Pattern1	Pattern 2

REFERENCES

- [1] Randal L. Schwartz, Tom Phoenix, Brian D Foy “Learning Perl” , 5th ed , O’Reilly Media, June 2008.
- [2] “Perl modules” which are used in the scripts needed for testcase automation are available at: <http://www.cpan.org/>
- [3] “The Perl programing Language” learned while writing Perl scripts can be known from: <https://www.perl.org/>
- [4] Balaji Subramanian and Wu-chun Feng “Understanding Power Measurement Implications in the Green 500 List”, In IEEE/ACM International Conference on Green Computing and Communications 2010.

TABLE III
RESULTS OF MODULE POWER CONSUMPTION

	Power Domain [V]			
(Nominal)	V1			
Real	X1V			
Pattern mode	Pattern1	Pattern2	Pattern3	Pattern4
Module name				
CPUx				
CPUy				
CPUz				
CPUi				
CPUj				
CPUk				
Module 0				
Module 1				
Module 2				
Module 3				
Module 4				
Module 5				
Module 6				
Module 7				
Module 8				
Module 9				
Module 10				
Module 11				
Module 12				
Module 13				
Module 14				
Module 15				
Module 16				
Module 17				
Module 18				
Module 19				
Module 20				
Module 21				
Module 22				
Module 23				
DUT type				
DUT device ID				
DUT ID laser mark				
DUT split				
DUT package variant				
Board ID				
Temperature deg C				
clk				
CPU mode				
Boot option				
Voltages V1				
Voltage - V2				