An Ultra Low Power High Accuracy Current-Mode CMOS Squaring Circuit

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***Abstract*— A new current-mode squaring circuit that can be used as a basic building block in analog signal processing systems is proposed. The design is based on MOS operating in the subthreshold region to assure low voltage and low power consumption. The performance of the design was confirmed by HSPICE simulation in 0.18μm CMOS process. The circuit is operated by ±0.7V supply voltage and consumes 0.2μW and maximum linearity error of 1.4%.**

***Index Terms*—Weak inversion, Squaring Circuit, Translinear principle**.

I. INTRODUCTION

Squaring circuit is a mathematical function that is widely used in communication system and measurements such as frequency doublers, peak amplitude detector, and analog multiplier [1-6]. Squaring circuits are also widely used in other practical applications such as RMS-to-DC converters in instrumentation and non-linear signal generation in analog signal processing. Low power supply consumption has become one of the main issues in electronic industry for many product areas such as cellular telephones, portable computers, neural network, wireless sensor network, and biomedical implants.

For ultra low power applications, it is more promising to focus on current-mode, which can be scaled from pA to μA levels. One good choice to achieve this requirement is the use of the MOSFET operating in the subthreshold region.

Most squaring circuits are based on the squaring feature of CMOS operating in strong inversion. Although the analog multipliers can achieve the same function, such circuit topologies tend to be more complicated [7] and aren't classified as an ultra low power circuits.

Some others are based on the Translinear Principle (TL) which is very useful in today's electronics era.

Many circuits have been implemented based on this principle using BJTs and MOS transistors in strong and in weak inversion regions [9, 10]. A family of a very low-power and low-voltage analog building blocks that are based on MOS translinear loops has been presented in [11] and references cited therein. They have utilized the bulk inputted configurations which are area efficient. However, the major drawbacks of these circuits are the devices mismatch and the limited gate-bulk operating voltage. Among the literatures reported, Carlos and Antonio proposed a current-mode squarer/divider circuit [12] based on the CMOS translinear loop. However the circuit operates from 1.5V and consumes 150μW. Abdelrahma, et.[13] and Wiegerink [14] have implemented squaring circuit using MOS transistors in strong inversion. The proposed circuit yields an output current expression with additional terms, to be compensated for, and it is not suitable for ultra low power applications.

In this paper, a new current-mode squaring circuit using the MOSFET operating in the subthreshold region is proposed. The circuit is suitable for ultra low power applications. The paper is organized as follows. Section II presents the proposed squaring circuit and its mathematical analysis. Simulation results and discussion are presented in section III. The paper conclusion is presented in section IV.

II. PROPOSED CIRCUIT

The proposed current-mode squaring circuit is shown in Fig1. With reference to Figure1, and by applying mixed TL (2PMOS + 2NMOS) through M1, M2, M3 and M4, then;

$$V_{gs1} + V_{gs4} = V_{gs2} + V_{gs3} \tag{1}$$

For MOS operating in subthreshold with the drain current is given by[16]:

$$I_D = I_{Do}.e^{\frac{V_{gs}-V_{TH}}{nv_t}} \tag{2}$$

$$V_{gs} - V_{TH} = nv_t \ln\left(\frac{I_D}{I_{D0}}\right) \tag{3}$$

Where, $I_{DO} = 2n\mu_n C_{ox}\frac{W}{L}v_t^{\,2}$ is the leakage current, n is the slope factor and $v_t = \frac{KT}{q}$ is the thermal voltage and K is Boltzman Constant.

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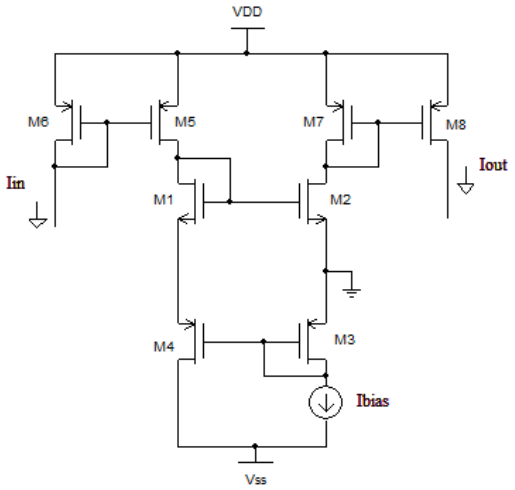

Fig.1 Proposed Squaring Circuit

To assure the MOS is operating in weak inversion, $I_D \le I_{Do}$ and $V_{DS} \ge 4v_t$ to assure forward saturation operation.

With $(W/L)_1 = (W/L)_2$ & $(W/L)_3 = (W/L)_4$, it is easy to show that;

$$I_{D1}.I_{D4} = I_{D2}.I_{D3} \quad (4)$$

But $I_{D1} = I_{D4} = I_{IN}$ and $I_{D2} = I_{out}$

I_{D3}, is the same as the bias current, I_{bias}. The output current is given by:

$$I_{out} = \frac{(I_{IN})^2}{I_{bias}} \quad (5)$$

Equation (5) shows that the output current is proportional to the square of the input current.

Simulation Results and discussion

Simulation was carried out using HSPICE simulator level 49 in 0.18 µm CMOS process. The supply voltages are $V_{DD} = -V_{SS} = 0.7V$ and the bias current, I_{bias}=100nA. Plots of the simulated and the calculated results are shown in Figure. 2. It is very clear that simulated and calculated results are in a good agreement with a maximum linearity error of 1.45 %. Plot of linearity error is shown in Figure. 3.

It is evident from the plot that the proposed circuit has a high accuracy.

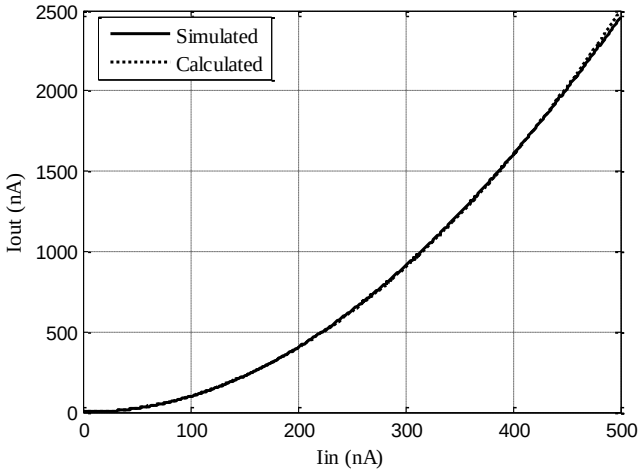

Fig.2 DC Transfer characteristics of squaring circuit

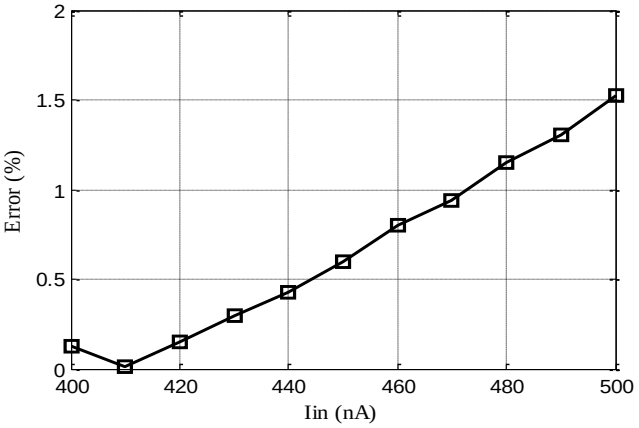

Fig3. Linearity error for the proposed circuit

For transient response, a triangle signal is applied with peak current of 50nA. The simulation result confirms the functionality of the circuit as shown in Fig4.

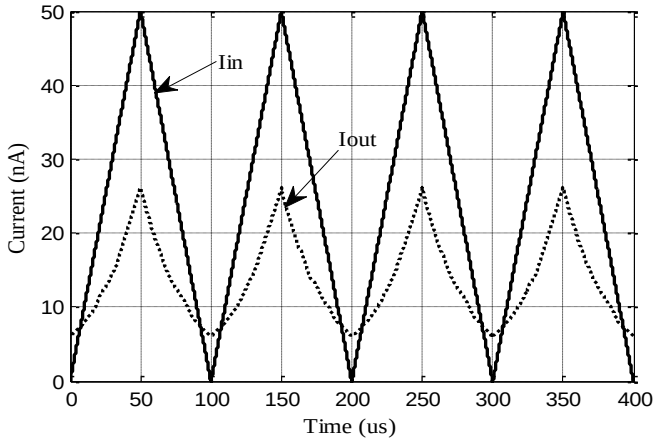

Fig.4 Triangular response for the proposed circuit

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Comparison between the performances of the proposed squaring circuit and the one proposed in [13] is summarized in table1.

Table1. Performance comparison

	Performance	
	Ref [13]	Proposed
Process	0.18um CMOS	0.18um CMOS
Supply Voltage	500mV	±700mV
Linearity error@ Iin=250 nA	13-14%	0.9%
Dynamic range	__	500nA
Power consumption	__	0.2 µW

It is evident from the above table that the proposed circuit has a better accuracy over dynamic range.

IV. CONCLUSION

This work proposed a low-voltage and low-power Current-Mode CMOS squaring circuit. The proposed circuit can be a useful building block in analog signal processing. The realization technique is based on the principle of the translinear characteristic. It is simple, has low power consumption property as advantage, and very suitable for implementation in integrated circuit form. HSPICE simulation results have been employed to confirm the performance of the proposed circuit.

We are continuing our work to modify this circuit somehow to increase its dynamic range further and improve its performance as well and results will be carried out in coming weeks.

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